OPEN HARDWARE COLLABORATION: A WAY TO IMPROVE EFFICIENCY FOR A TEAM

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Abstract

SOLEIL is a third generation Synchrotron radiation source located near Paris, France. Today, the Storage Ring delivers photon beam to 26 beamlines. In order to improve the performance of the machine and beamlines, new electronics requirements have been identified. Up-to-date commercial products are preferred but sometimes customs hardware designs are essential. At SOLEIL, the electronic group comprises a team of eight people in charge of the design, implementation and maintenance of the control and data acquisition electronics for the beamlines and accelerators. A large electronics installed base and a small team mean that we have very little time left to focus on the development of new hardware designs. As an alternative, we focus our development around the Open Hardware [1] (OHWR) initiative from CERN, dedicated for electronics designers at experimental physics facilities to collaborate on hardware designs. Starting in 2010, we studied how we could be more active on OHWR. After checking a few legal aspects about the OHWR and the feasibility of sharing source file designs, we now collaborate as an evaluator and a contributor. As a contributor, we share some boards in the SPI BOARDS PACKAGE project [2] that we have developed to face some current challenges at SOLEIL. As an evaluator, SOLEIL collaborates with characterizations of the TDC core project [3], and plan to evaluate FMC carrier. This approach allows us to be more efficient with development. We will present our approach, the issues that we have to face, and the benefits we obtain.

SOLEIL APPROACH

For the SOLEIL electronics group, being active on OHWR is a new approach to collaborate with other institutes, promoting our developments and evaluating projects available on OHWR. It is extremely beneficial to be able to exchange information on the site with up to eleven institutes leading different projects. It is interesting to see the number and variety of projects increasing quickly with up to 100 projects shared on the site. OHWR also has the support of 16 commercial companies who develop, produce and/or test open hardware products. It is also a good model for industrialization of the products.

Before taking an active role on OHWR, three years ago we checked various aspects, regarding compatibility with our electronic CAD licence from Europractice to share our designs, and regarding the content of the OHWR licence; we were also awaiting feedback from other institutes. SOLEIL has now bought a commercial Cadence licence which enables us to share our design source files under the OHL licence.

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EXPECTATIONS

SOLEIL is active on OHWR evaluating the TDC core and sharing design source files in the SPI Boards Package project, see Fig. 1. The next issue for the acquisition activity of the electronics group will be the evaluation of FMC boards as illustrated below.

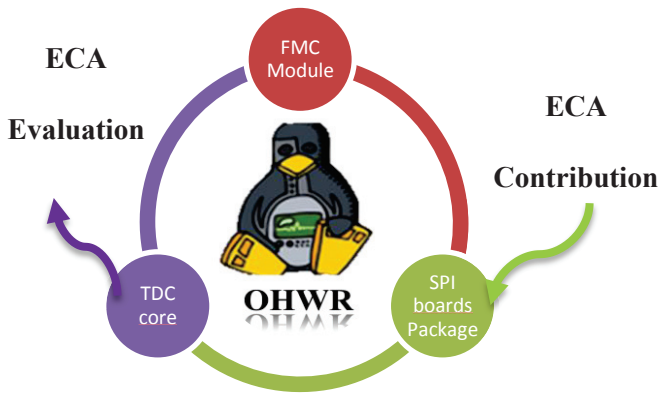

Figure 1: Functional diagram of SOLEIL activity on OHWR.

From a technical point of view, SOLEIL expects that OHWR will enable it to develop in a collaborative manner with design reuse and to improve the products developed in house through feedback and peer review with other institutes. In term of collaboration, we believe that this platform will allow us to promote and share projects with the community. Moreover, the presence of commercial companies on OHWR encourages collaboration with industry, especially to facilitate production of hardware for evaluation as well as off-the-shelf products.

Finally, in terms of manpower, the strategy to use OHWR for our team is to reduce the development cycle, the hardware production cycle and keep working with limited resources.

EVALUATION FROM OHWR

In its technological watch activity, SOLEIL evaluates solutions available on the Open Hardware Repository. The first project evaluated is the TDC Core. It provides a time to digital converter core for XILINX [4] Spartan-6

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FPGAs (Fig. 2) with a measured precision of ±52 ps and a typical range of 268 ms. Being involved in such a project has many advantages with portable and flexible source code leading to a low-cost TDC solution, independent of market constraints. The goal of this evaluation is to complement industrial products and to propose an open-source alternative TDC to users.

The TDC core project is a high precision (sub-nanosecond) time to digital conversion core for Xilinx Spartan-6 FPGAs. It timestamps the events represented by the edges of signal inputs. The user can define whether rising or falling or both edges of the incoming signal to be time stamped.

This project provides a demonstration system which includes the following IP cores: a Lattice LM32 Microprocessor (command line interpreter), a Wishbone bus and basic peripherals. The TDC Core can therefore be controlled via a serial link using a command line shell. All elements are open source from OHWR.

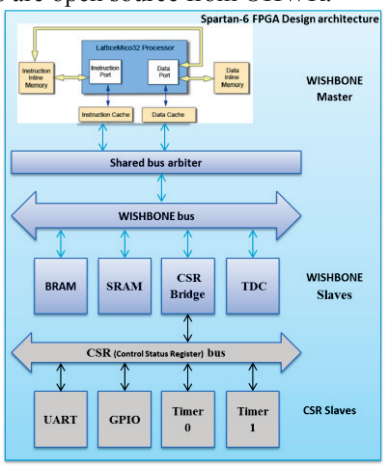

Figure 2: Demonstration design architecture.

To evaluate the performance of this TDC system, the first series of tests have been implemented in the laboratory on an evaluation platform as shown on Fig. 3, with a Xilinx SP605 board and a FMC DIO 5-channel daughterboard which is also open source from OHWR.

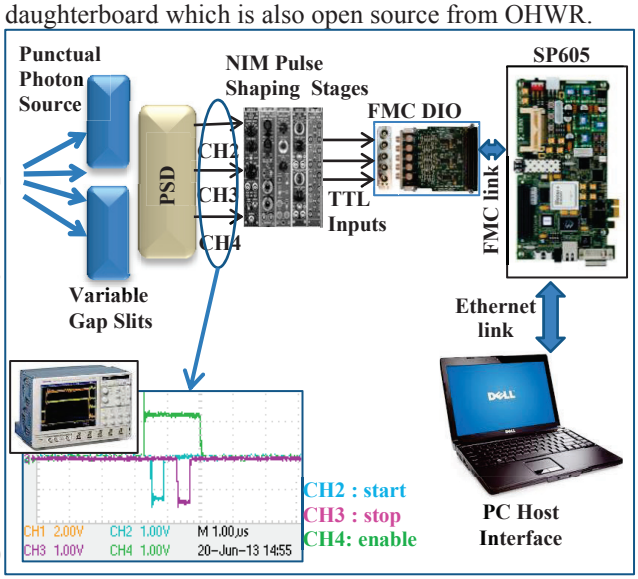

Figure 3: First tests on Sirius detector.

We obtained first results on an X-ray PSD (Position Sensitive Detector) gas filled detector used by the SIRIUS Beamline [5] as described in the figure below. Such detectors deliver two impulsions (start and stop) occurring at time t_{start} and t_{stop}. The difference t_{start}-t_{stop} is directly proportional to the position at which the detected photons impinge on the detector. The TDC's role is to measure and build the histogram of positions for a given sampling. Start and Stop signals are validated by a gate signal delivered by the detector. Figure 4 shows that for two different openings of a slit in front of the detector entrance windows, the obtained histograms are different. This shows that the TDC core associated with the detector is able to locate the photon source. With a fully exposed detector (histogram on the left) measurements we measured a peak-peak histogram of 500 ns. This falls to 200 ns when the slit gap is reduced down to 1 cm (histogram on the right).

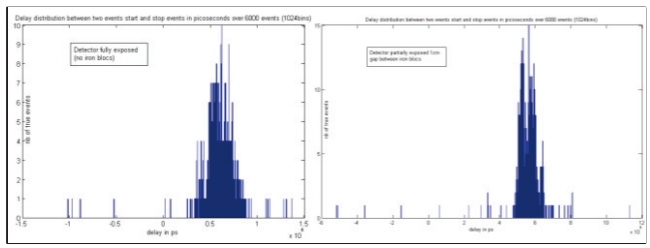

Figure 4: First results on Sirius detector.

The TDC system has a typical measurement range of 268 ms encoded in 38 bits of which 1 LSB corresponds to 0.98 ps. A typical dead time of 48 ns has also been achieved and measured. That was possible by implementing a double buffering process which was not initially present in the source code.

Based on what we obtained from the OHWR TDC Core project, we have customized it for our own requirements, adding some new features.

We initially tested this core on a Xilinx evaluation board, we also migrated this TDC core to the SPEC board [6] (Simple PCI Express Carrier board). The FMC PCIe Carrier is an FMC mother board with PCIExpress form factor that can hold one FMC card.

Communication with the board was initially developed on a USB link. We implemented a UDP Ethernet bridge giving more flexibility and easier integration to our control framework. That was done by using the IPBus project from OHWR which implements an Ethernet packet handle machanism supporting ARP, ICMP and UDP/IP protocols. We were also able to communicate via an SFP port by using a RJ45 to SFP converter and implementing a MAC to SFP layer from Xilinx cores.

In order to improve data rate acquisition we are currently working on the implementation of DDR3 RAM in the project.

As feedback for OHWR, we shared our evaluation results in the TDC Core OHWR project. This evaluation not only achieved good results on this platform but also gave us a first experience on OHWR as evaluators. It also

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demonstrates that this way of working significantly reduces the project development cycle and resources and promotes collaborative work and design reuse. First tests on a detector on SIRIUS beamline have been performed and gave good results.

CONTRIBUTION TO OHWR

As a contributor, SOLEIL is present on OHWR with the SPI Board Package project. This project presents and shares information about electronic boards developed by the SOLEIL electronics group and application notes describing how this set of boards is used in synchrotron applications.

The boards already available in the repository are:

- SPICONTROLLER: controller board based on ARM [7] Cortex M3 microcontroller.
- SPIETBOX: Processing encoder signal board based on Xilinx FPGA, 4 Encoder inputs/outputs, 4 TTL Outputs, 1 SPI interface.

For each board, the SVN repository gives access to schematic, GERBER and firmware source files which are shared under CERN OHL V1.1 licence.

SPICONTROLLER

SPICONTROLLER is the controller board for the SPI Boards Package. It manages a task for communication with the control system via Ethernet and with modular boards via an SPI interface. Moreover, it enables specific algorithms to be embedded into the controller.

The main features and the architecture of the boards, as shown on Fig. 5, are presented on the wiki page of the site.

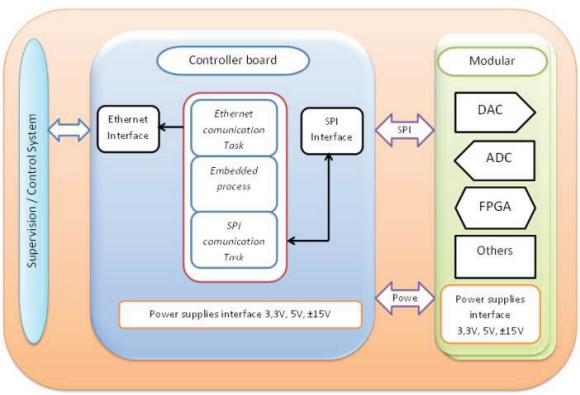

Figure 5: SPI Boards architecture.

Recently application notes about the use of this architecture at SOLEIL have been added. They describe the architecture implemented for the analogue feedforward (FFWD) of electromagnetic insertion devices [8] such as EMPHU or HU640. This development, the architecture of which is presented in Figure 6 contributes in the improvement of beam orbit stability.

The process to control undulators is embedded at low level in the microcontroller. It manages the FFWD, generating analogue signals synchronously to drive undulator power supplies. Moreover, the SPICONTROLLER platform allows a faster control of power supplies enabling (5 Hz) switching of magnetic fields use for Dichroism experiments. In this architecture, TANGO [9] high level software is used to configure the SPICONTROLLER.

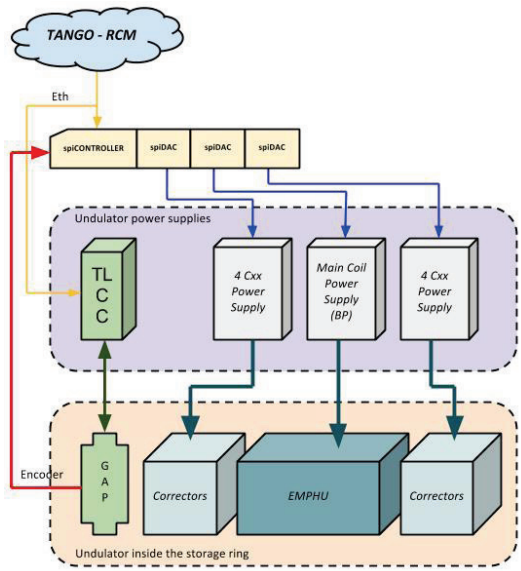

Figure 6: EMPHU control architecture.

SPIETBOX

SPIETBOX is the processing board developed around an FPGA in order to process incremental and SSI encoders. Figure 7, below, presents the architecture of the board.

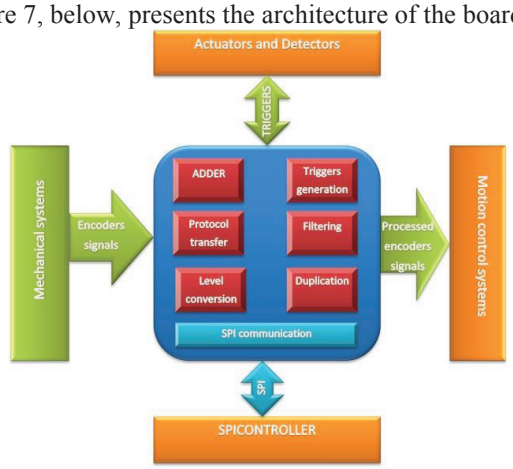

Figure 7: SPIETBOX Architecture.

This board, which can operate standalone or connected to a SPICONTROLLER, can embed the following process:

- Adding 2 TTL Encoders (For eccentricity compensation of a mechanical axis)

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- RS422 to TTL level conversion
- Duplicate encoder signal
- Generation of triggers from an encoder signal
- Protocol transfer SSI 12 Bits to SSI 25 Bits, Quadrature to PULSE and DIR signals

One application of the SPIETBOX is for synchronized acquisition during continuous scanning. One implementation is on the PX1 beamline [10], to synchronize a Goniometer with Pilatus detector in order to build the shape of protein molecules in 3D.

The following architecture, Fig. 8, has been implemented. It synchronizes goniometer position, Shutter aperture and Pilatus acquisition. It allows the acquisition of frames on the Pilatus detector during goniometer movement.

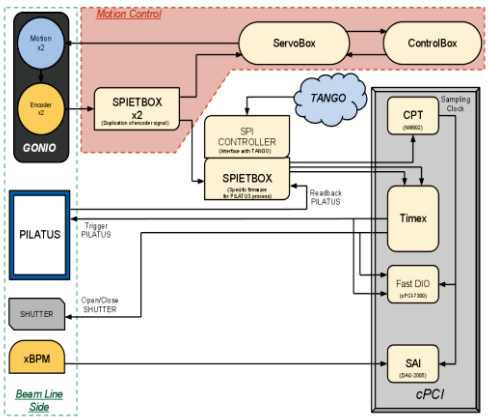

Figure 8: Architecture for PX1acquisition with Pilatus.

The Pilatus detector allows four acquisition modes, i.e. four different ways to synchronize acquisition. In this architecture these synchronizations are implemented in the SPIETBOX, managing the following signals: encoder position, trigger to and from the Pilatus, shutter trigger.

The SPICONTROLLER is used to configure the different modes and to transfer some information along the process. The information coming from the SPIETBOX and the beam intensity from XBPM are logged for diagnosis along the process.

At the moment in the most used acquisition mode, the SPIETBOX sends a trigger to start the PILATUS detector which uses its own internal clock to take the images, see Fig. 9.

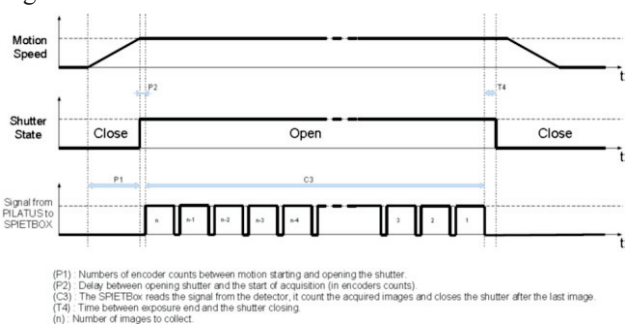

Figure 9: Timing of the most use triggering mode.

The advantages of hardware synchronization using the SPIETBOX are the good correlation between data acquisition and motor position. Moreover, it enables the scientists to have a quick validation of the acquisition and fast access to information, thanks to the logging of all experimental conditions. Lastly, it simplifies control of the Pilatus detector's modes.

CONCLUSION

The progress made at SOLEIL to organize our activity on OHWR took time, and continues to require lobbying to convince SOLEIL management as this model of collaboration is always complex. Nevertheless we are now active as contributor and evaluator.

As a contributor, feedback to improve our contribution has not so far been at the expected level. Our analysis is that organizing legal aspects in order to share our source files took time and people had used alternative solutions to reach the same functionality. However we are still convinced that collaboration requires a legal framework for sharing source files such as that provided by OHWR.

As an evaluator, the first experience is encouraging, and allowed our team to be more efficient and save time on TDC implementation.

Nevertheless, even if the collaboration worked well, we notice that technical support is made on a best effort basis and some designs committed on the repository need debugging. The support or the collaboration in this case is varied.

For the future we are prospecting on up to date acquisition platforms. In this approach FMC (FPGA Mezzanine Carrier) carriers are interesting for evaluation.

Finally, OHWR is a good way to facilitate collaboration, sharing news through mailing lists or announcements on the website for the entire community.

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