A DESIGN OF SUB-NANOSECOND TIMING AND DATA ACQUISITION ENDPOINT FOR LHAASO PROJECT

Weibin Pan#, Qiang Du, Guanghua Gong, Hongming Li, Jianmin Li
Department of Engineering Physics, Tsinghua University, Beijing, 100084 China
Key Laboratory of Particle & Radiation Imaging (Tsinghua University), Ministry of Education

Abstract

The particle detector array (KM2A) of Large High Altitude Air Shower Observatory (LHAASO) project consists of 5631 electron and 1221 muon detection units over 1.2 square km area. To reconstruct the incident angle of cosmic ray, sub-nanosecond time synchronization must be achieved. The White Rabbit (WR) protocol is applied for its high synchronization precision, automatic delay compensation and intrinsic high band-width data transmit capability. This paper describes the design of a sub-nanosecond timing and data acquisition endpoint for KM2A. It works as a FMC mezzanine mounted on detector specific front-end electronic boards and provides the WR synchronized clock and timestamp. The endpoint supports EtherBone protocol for remote monitor and firmware update. Moreover, a hardware UDP engine is integrated in the FPGA to pack and transmit raw data from detector electronics to readout network. Preliminary test demonstrates a timing precision of 29ps (RMS) and a timing accuracy better than 100ps (RMS).

INTRODUCTION

The Large High Altitude Air Shower Observatory (LHAASO) [1] is proposed to build a 1.2 km^2 complex ground detector array at Shangri-La of Chain. The square KM complex detector array (KM2A) of LHAASO consists of 5631 electron and 1221 muon detection units, aiming to precisely reconstruct the air shower events with high angular resolution. It puts forward a big challenge to the timing distribution system which should be capable of synchronizing more than 6000 nodes with a resolution of 0.5 ns (RMS).

Recently an Ethernet based synchronization protocol called White Rabbit [2] is proposed, aiming to achieve a timing precision of tens of picoseconds and sub-nanosecond accuracy for large distributed systems. It shows a great applicability to the LHAASO project for its capability of synchronizing large number of nodes and outstanding timing performance [3-4]. Moreover, it is fully compatible with the standard gigabit Ethernet, which provides a cost-effective solution that combines timing distribution and DAQ function over the same physical link.

Based on the White Rabbit technology, a prototype of timing and DAQ network of LHAASO is proposed. Preliminary test has been performed to evaluate the timing performance under multistage cascade topology

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pwb.thu@gmail.com

WHITE RABBIT NETWORK IN LHAASO

The timing and DAQ network of LHAASO shown in Fig.1 [4] consists of cascaded WR switches and WR nodes. The WR switch recovers the synchronized clock and timestamp from the upstream and distributes them to another WR switch or a WR node. In addition, the WR switch serves as a standard gigabit Ethernet switch in the DAQ network. The timing and data links share the same optical fiber media.

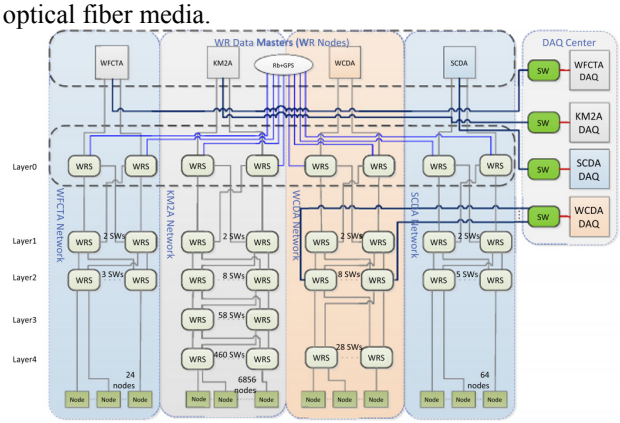

Figure 1: Topology of LHAASO timing and DAQ network.

We assume that the WR switches applied in the LHAASO have 18 ports (e.g. WRS v3.3 [5]), two of which are connected to two different switches of upper layer for redundancy, and the other 16 ports are used as downlink ports. In the KM2A network, 460 WR switches are required in the layer 4 to support 6,856 nodes. Only 15 downlink ports of each switch are occupied, with one backup port reserved.

DESIGN OF THE CUTE-WR

In the LHAASO, WR nodes are integrated with different frontend electronics of more than 6,000 detection units. A compact universal timing endpoint based on the White Rabbit (CUTE-WR [6]) is developed. It implements the WR PTP core with minimum components required. The DAQ and slow control functions are also implemented in the CUTE-WR.

Hardware

The CUTE-WR, as shown in Fig.2 [6], is a FMC daughter card that can be integrated with any custom circuits. It can be treated as a network interface with sub-nanosecond timing support. The FMC connector on the CUTE-WR provides synchronized time information and a bidirectional FIFO-like interface for the carrier board.

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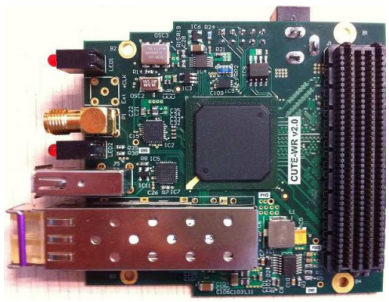

Figure 2: The White Rabbit Node: CUTE-WR.

Timing Interface

The synchronized clock, PPS signal and UTC timestamp are transmitted to the frontend electronics in LVDS standard. To save pin resource, the PPS and UTC are serialized as pps_utc. The data format is shown in Fig.3.

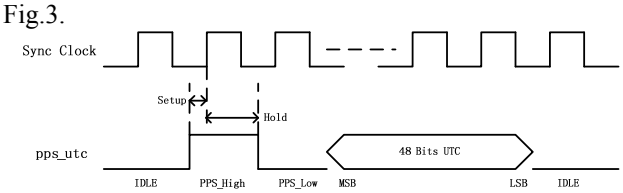

Figure 3: Data format of timing interface.

The frequency of provided clock can be customized, and is set to 125 MHz by default. The pps_utc is synchronized to the clock with sufficient setup and hold time. It holds the logic 0 level until the PPS signal is triggered. Then a data set is made up of three parts: pps_high bit, pps_low bit and 48 bits utc timestamp. The pps_high bit indicates the start of one second while the utc timestamp represents current time in seconds.

DAQ and Slow Control

Experimental data produced in the frontend electronics can be transmitted to the remote date center through White Rabbit network. Besides, slow controls can also be performed through the Ethernet. As a network interface, the CUTE-WR is completely transparent to the frontend electronics except for an optional hardware based UDP engine, which can be enabled to pack and extract raw data for frontend electronics.

Data communication between the CUTE-WR and frontend electronics is implemented with a carrier-to-mezzanine (C2M) interface and a mezzanine-to-carrier (M2C) interface as shown in Fig.4.

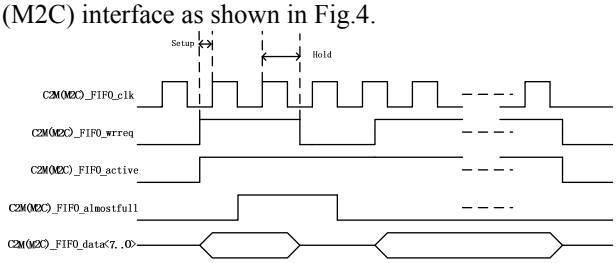

Figure 4: C2M and M2C FIFO-like interface.

The 125 MHz FIFO clock and 8 bit data bus enable the maximum transfer rate of 1000 Mbps. FIFO_wrreq and FIFO_active indicate the valid byte and valid packet respectively. FIFO_almostfull is used to stall the transmission.

The slow control for the CUTE-WR itself is performed with a network layer of the Wishbone bus called EtherBone [7]. It is a bridge between Ethernet and on-chip Wishbone bus, and hence enables the access to internal registers of the CUTE-WR. Benefiting from the EtherBone, many functions such as remote firmware update and remote monitor can be implemented.

The data flow of the CUTE-WR is illustrated in Fig.5. Incoming packets are classified and distributed to three categories: PTPv2 packets are routed to a LM32 processor through a Mini-NIC; EtherBone packets are routed to an EtherBone slave core; packets for external circuits are routed to the FMC connector directly or through a UDP engine. Since the PTPv2 and EtherBone packets take very low bandwidth, data transfer for external circuits can achieve very high throughput, which is above 500 Mbps under preliminary test.

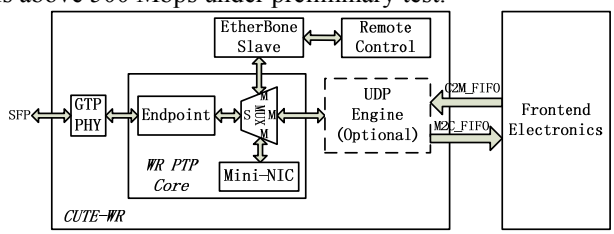

Figure 5: Data flow of the CUTE-WR.

DEMONSTRATION SETUP AND TEST

To evaluate the timing performance of the White Rabbit, a test environment including 4 WR switches and 6 CUTE-WRs has been built. The PPS skews between the grandmaster WR switch and all slave nodes are measured under different topology. Hence the synchronization precision and accuracy can be verified.

Synchronization Precision

Connect one of the CUTE-WRs (Slave) to a WR switch (Master) with a 2 km optical fiber. The PPS skew is measured by an oscilloscope and has a standard deviation of 21 ps as shown in Fig.6.

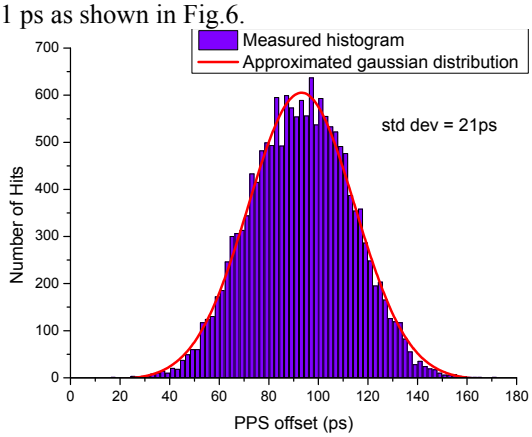

Figure 6: Histogram of PPS skew between WR switch and CUTE-WR.

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Accuracy of Parallel Topology

A parallel topology of WR switches is setup as shown in Fig.7. The mean value of PPS skew between the grandmaster and any node is interpreted as the accuracy of synchronization. The histogram of skew distributions for all the slave devices under different runs is shown in Fig.8.

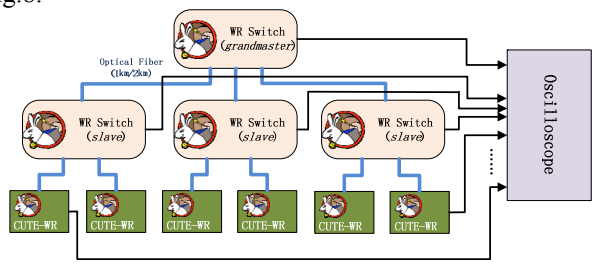

Figure 7: Parallel topology of WR switches.

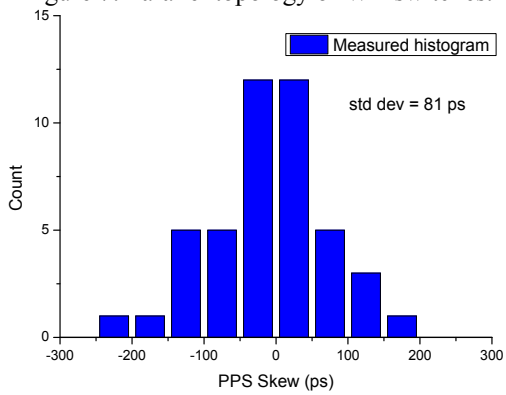

Figure 8: PPS skew distributions of parallel topology.

Accuracy of Cascade Topology

The cascade topology and corresponding PPS skew distributions are shown in Fig.9 and Fig.10.

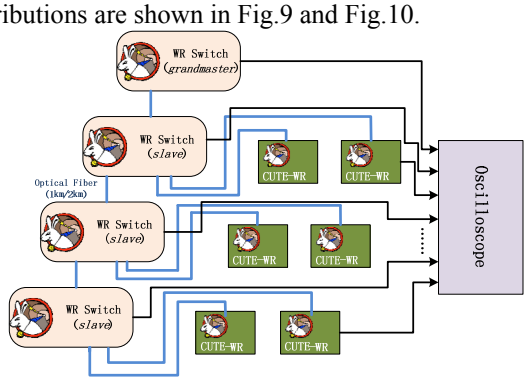

Figure 9: Cascade topology of WR switches.

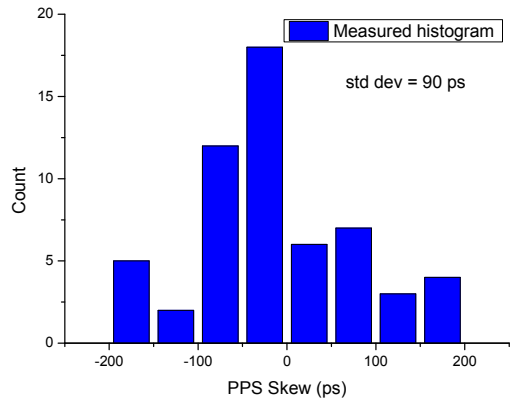

Figure 10: PPS skew distributions of cascade topology.

SUMMARY

The LHAASO project requires high precise time and clock synchronization among thousands of detectors nodes. A timing distribution network based on the White Rabbit protocol is proposed. A compact WR node called CUTE-WR is developed to provide sub-nanosecond timing and gigabit Ethernet interface for different frontend electronics. A test system including 4 WR switches and 6 CUTE-WRs is setup, and the timing performances under different topologies are evaluated. The PPS skew between WR switch and CUTE-WR achieves a precision of 21 ps, and PPS signals of all nodes are aligned within 100 ps (RMS).

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