CONTROL ENVIRONMENT OF POWER SUPPLY FOR TPS BOOSTER SYNCHROTRON

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Abstract

The TPS is a latest generation of high brightness synchrotron light source and scheduled to be commissioning in 2014. Its booster is designed to ramp electron beams from 150 MeV to 3 GeV in 3 Hz. The control environments based on EPICS framework are gradually developed and built. This report summarizes the efforts on control environment of power supply for TPS booster synchrotron.

INTRODUCTION

The TPS [1] is a latest generation of high brightness synchrotron light source which has been under construction at the National Synchrotron Radiation Research Center (NSRRC) in Taiwan since 2010. It consists of a 150 MeV electron Linac, a 3 GeV booster synchrotron, and a 3 GeV storage ring. Civil construction has started from February 2010 and the constructions are complete in this year. Accelerator system installation and integration will be proceeding in the late 2013. Commissioning with beam is scheduled in the late 2014. The EPICS (Experimental Physics and Industrial Control System) which is a set of open source software tools, libraries and applications developed collaboratively and used to create distributed soft real-time control systems for scientific instruments is chosen for the TPS accelerator control. Therefore, the TPS booster power supply should support EPICS for display creation, archiving, alarm handling and etc.

The control interfaces of TPS booster power supplies have two major categories: one is for the large main power supply which could provide current up to 1200 and 130 amperes and used for dipole and quadrupoles respectively; the other is small/medium power supply which supports 10 amperes current output and used for sextupole, correctors and bending trim coils. Table 1 summarizes the specifications of booster ring power supplies.

Table 1: TPS booster Ring Power Supply Summary

Magnet	Type	Max Current	Stability ppm	Number of PS	Vendor	Control Interface
Dipole	Unipolar	1200 A	±10	1	IE Power (Eaton)	Ethernet*
Quadrupole	Unipolar	130 A	±10	4	IE Power (Eaton)	Ethernet*
Sextupole	Bipolar	± 10 A	±10	2	ITRI	CPSC (Ethernet) with Waveform support in CPSC
Corrector	Bipolar	± 10 A	±10	HC: 60 VC: 36	ITRI	CPSC (Ethernet) with Waveform support in CPSC

All of these power supplies should have features of waveform play with trigger functionalities to enable electron beams ramp from 150 MeV to 3 GeV in 3 Hz. The large power supply provides Ethernet control interface and trigger input for waveform download and play. One dedicated EPICS IOC will be built to serve its control, monitor, and status display. The small power supply has a special designed EPICS IOC allocated at power supply rack for its control. The environments of these two power supply control will be summarized in this reports.

BOOSTER POWER SUPPLY STATUS AND CONTROL INTERFACE

The booster main power supplies are composed of one dipole power supply with maximum current 1200 Ampere and four family quadrupole power supplies with maximum current of 130 Ampere. The IE Power [2] initially won the bid and was contracted the project. But later it was acquired by Eaton. This complicates administrant process and caused the delivery delay. The power supply now is still under vender's test and modification phase the delivery is expected a half year later. These power supplies will be equipped with the same controller with serial control interface internally. Serial to Ethernet adapter will interface with control system. These power supplies will support external trigger and internal waveform generator for booster power supply ramping.

The small/medium power supply for booster corrector and sextupole is a sophiscated switching power supply with analogue regulator. It is designed by our power supply group and contratced to be manufactured by Industrial Techonology Research Institude (ITRI) [3].The power supply module will be also applied for TPS storage ring slow correctors, fast correctors, skew quadrupoles and etc. Each power suply sub-rack accomodates up to eight power supply modules. The center slot is allocated to install a special designed EPICS IOC with waveofrm play features.

The booster power supply EPICS IOC and GUI has been designed and tested before the power supply arrival. Fig. 1 shows the overall booster ring power supplies control interface. The most probably booster ramping waveform is sinusoidal wave. Two family of sextupole are driven by two small power supplies. There are 60 horizontal corrector and 36 vertical correctors. Corrector power supplies of the booster will adopt CPSC also. If corrector ramping is necessary, the CPSC has built-in waveform generator which can fulfil this functionality.

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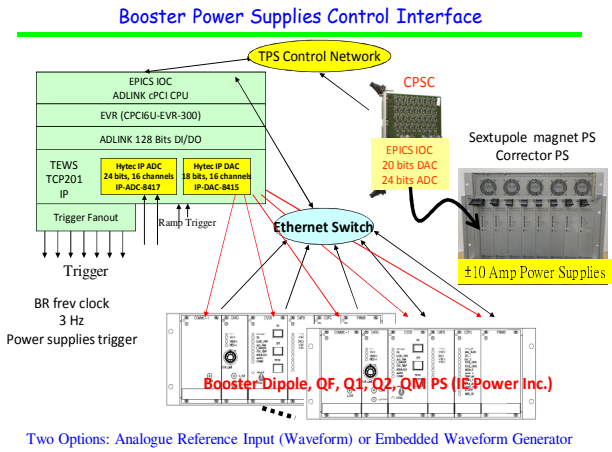

Figure 1: Control infrastructure of TPS booster ring power supplies.

MAIN POWER SUPPLY WAVEFORM CONTROL INTERFACE

To support electron beams ramping from 150 MeV to 3 GeV, Maltab-based GUI (graphic user interface) is proposed to generate waveform and download to EPICS IOC via Matlab EPICS channel Labca. Fig. 2 shows the preliminary GUI for booster bending magnet and 4 families of quadrupoles ramping waveform generation and download. It could support three operation modes: (1) DC injection (2) on-the-fly symmetry sine (3) on-the-fly asymmetry sine. The injection time (Tinj), extraction time(Textr), waveform maximum and minimum value could be adjusted according to beam condition to acquire the optimum waveform for ramping. Fig. 3 shows the tracking error which is critical to booster ramp tuning. The pink line shows the tracking error for magnet readings difference to bending magnet settings and the blue line is magnet reading difference to magnet themselves settings. Because the booster main power supply has not yet delivered, Fig. 3 shows the temporary simulated power supply current readings/settings where the AO channels is connected directly to AI channels.

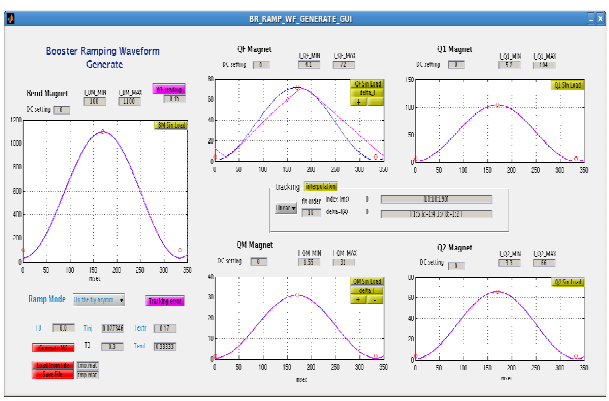

Figure 2: GUI for booster bending magnet and 4 families of quadrupoles ramping waveform generation and download.

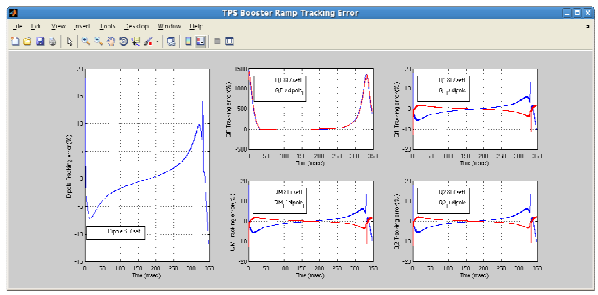

Figure 3: The tracking error for magnet readings difference to bending magnet settings (red line) and to magnet themselves settings (blue line) respectively.

CORRECTOR POWER SUPPLY CONTROL INTERFACE

To support diverse functionalities of fast orbit feedback [4], booster ramping, compensations for insertion device and skew quadrupoles, the corrector power-supply controller (CPSC) for TPS corrector power supply is proposed. It is embedded with ARM processor and Xilinx Spartan-6 FPGA and was contracted to D-TACQ [5]. This module will be installed at center slot of the power supply sub-rack to isolate ambient noise from cablings and simplify power-ground complications to achive high stability. The module embedded EPICS IOC and FPGA supports slow access for the EPICS CA clients and fast settings from orbit feedback system. The functional block diagram of CPSC module is shown in Fig. 4.

There are 60 horizontal and 36 vertical correctors installed on TPS booster. These correctors require 12 CPSCs to control their power supply modules. EDM control pages had been developed and provided as Fig. 5. It includes signal trend, waveform display, synchronization mode settings and etc.

Besides, there is one extra CPSC for two families of sextupoles and bending trim coils. Fig. 6 shows GUI for booster 2 families of sextupoles and bending trim coil ramping waveform generation and download.

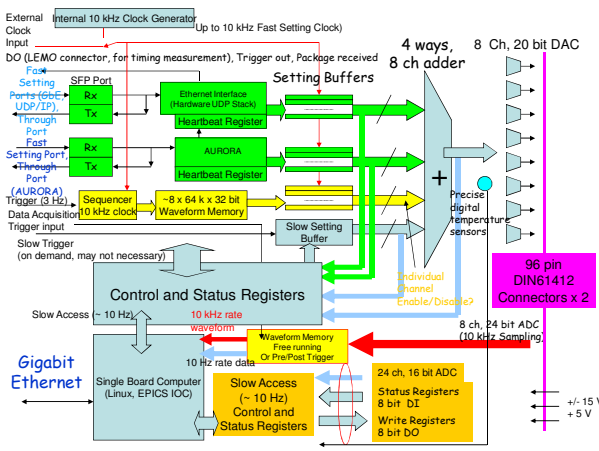

Figure 4: Functional block diagram of the corrector power supply controller (CPSC) module. It includes fast setting from orbit feedback, slow setting and waveform download from EPICS CA.

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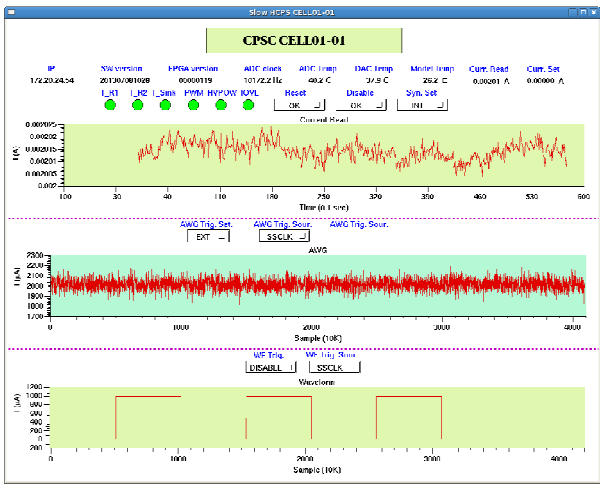

Figure 5: GUI for booster corrector controller (CPSC) control EDM page.

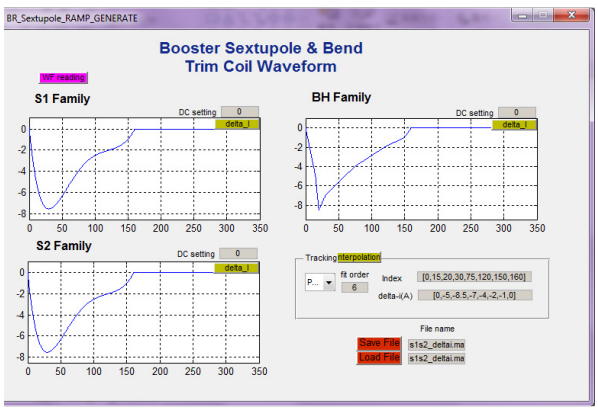

Figure 6: GUI for booster 2 families of sextupoles and bending trim coil ramping waveform generation and download.

Preliminary Corrector Power Supply Testing

The power supply achieves 20 bit performance where it is equivalent to 1 nrad resolution for slow correctors which provide around 600 urad kick strength and 0.05 nrad for fast correctors which provide around 30 urad kick. Noise level is around -120 dB and it is equivalent around 1uA. Furthermore, the fast corrector response is corresponded to the 1.3 kHz bandwidth. The test results are shown in Fig. 7 and Fig. 8.

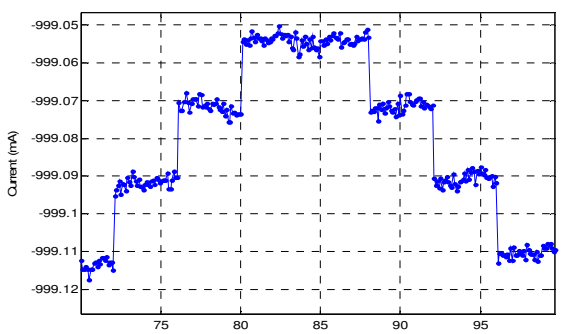

Figure 7: 20 bit performance, each step is around 20 uA.

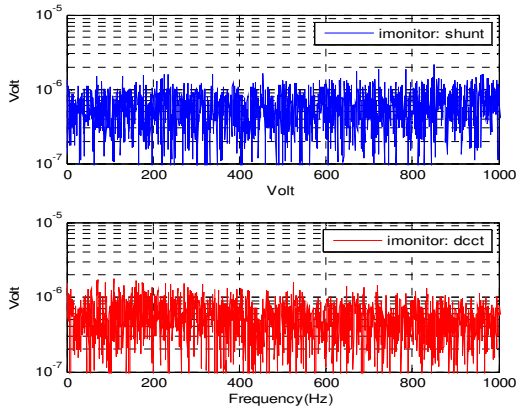

Figure 8: Noise level is around 1uA.

Built-in waveform functionality is also supported for orbit correction during the booster ramping. The slow setting synchronized mechanism by externally trigger is also provided and test as Fig. 9. The red line is setting value and blue line is reading value that is actually changed when triggered (the green line).

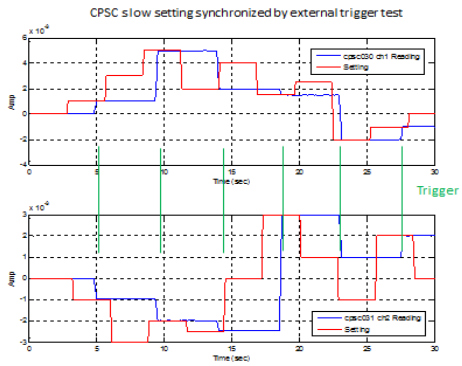

Figure 9: CPSC synchronized slow setting test.

SUMMARY

Preliminary user interfaces and operation procedures of booster power supply are presented in this report. Before power supplies delivered, the power supply control environment was constantly established for developing the operation applications in advance. The operation applications including the operation interface, power on/off setting and checking, waveform download and etc. will be continuously developed.

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