STATUS OF THE TPS TIMING SYSTEM

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Abstract

Implementation of timing system of the Taiwan Photon Source (TPS) is underway. Timing system provides synchronization for electron gun, modulators of linac, pulse magnet power supplies, booster power supply ramp trigger, bucket addressing of storage ring, diagnostic equipments, beamline gating signal for top-up injection, synchronize for the time-resolved experiments. The system is based on event distribution system that broadcasts the timing events over optic fibre network, and decodes and processes them at the timing event receivers. The system also supports uplink functionality which will be used for the fast interlock system to distribute signals like beam dump and post-mortem trigger with less than 5 μsec response time. Software support is in preceded. Time sequencer to support various injection modes has been developed. Timing solutions for the TPS project will be summarized in the following paragraphs.

INTRODUCTION

The TPS is the latest generation synchrotron light source under construction and commissioning is planned in 2014. Event based timing system will be applied for TPS [1-4]. Implementation of timing system is in proceeding. The test system had been already applied for the TPS 150 MeV linear accelerator (linac) commissioning and acceptance during the second quarter of 2011. Various supports for the timing system are in preparation.

The timing system is based on the events coming from event generator. EVG handles the accelerator synchronization and trigger the injection and the extraction pulse devices. In order to provide an efficient management of the sequence RAM in the event generator, the sequencer design of timing system is on going.

EVENT BASED SYSTEM FOR TPS PROJECT

The TPS timing system is an event based system. A central EVG generates events from an internal sequence RAM and external sources [5]. These events are distributed over optic fiber links to multiple event receivers (EVRs) [6]. The EVRs, which are located in the control system interface layer, decode the events referred to as hardware triggers or software interrupts. For the linac, the decoded events are further encoded by a gun transmitter and sent over a fiber link to the gun high voltage deck. The external event sources include pulse per second (PPS) signal which is locked to global positioning system (GPS), AC mains 60 Hz trigger, post-mortem trigger after beam loss and machine protection system

activated. The event clock is derived from the 499.654 MHz master oscillator so that it is locked to the RF frequency. The master oscillator can be locked to external reference from a GPS disciplined Rubidium 10 MHz clock. TPS timing modules with 6U CompactPCI form factor modules include cPCI-EVG-300, cPCI-EVR-300, cPCI-EVRTG-300 and linac gun trigger receiver. Adopting PCIe-EVR-300 to accompany with fanless embedded EPICS IOC for some applications is also supported. Configuration tools were developed. Save and restore supports are also available. Sequencer design is current work. Installation of the system is scheduled in early 2014.

ACCELERATOR TIMING

A prototype of sequence control by EPICS sequencer was tested. The timing sequence control is based on state machine. The timing sequencer will manipulate several PVs to define the transition among different states and communication with the other IOCs. The sequence RAM will be disabled by the stop interrupt of the sequence RAM and replaces sequence RAM contents.
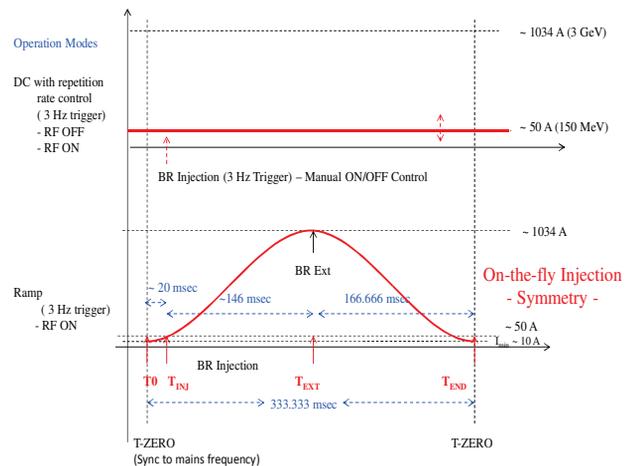

Figure 1: Booster synchrotron power supply waveform plans.

The TPS accelerators will be operated in 3 Hz repetition rate. The booster power supply could be operated in DC mode or ramping mode with on the fly injection. The booster ring can work like storage ring in DC mode of booster supply. It will help to check booster equipment and parameters through beam which is from linac can survive at booster ring. The on the fly injection mode provide flexibility for the booster tuning ramping performed just active ramp trigger as shown in Fig. 1.

The sequence is started at T-ZERO which is the trigger time of the sequence RAM and start time of a new accelerator cycle. Energy ramping time of the booster synchrotron is about 150 msec when repetition rate set at 3 Hz. The sequence RAM will stop after the booster synchrotron finish the ramping cycle. There are more than 100 msec time window available for change contents of the sequence RAM. Using EPICS sequencer to program sequence RAM after the sequence RAM stop. The timing sequencer running in the timing master EPICS IOC for sequence RAM control in machine operation is satisfied. All parameters for the machine operation modes will be designed as specific EPICS PVs, such as operation mode, e-gun mode (single bunch or multi-bunch), bucket address, repeat cycle, top-up injection, decay mode and etc. Timing sequencer structure is presented in Fig. 2.
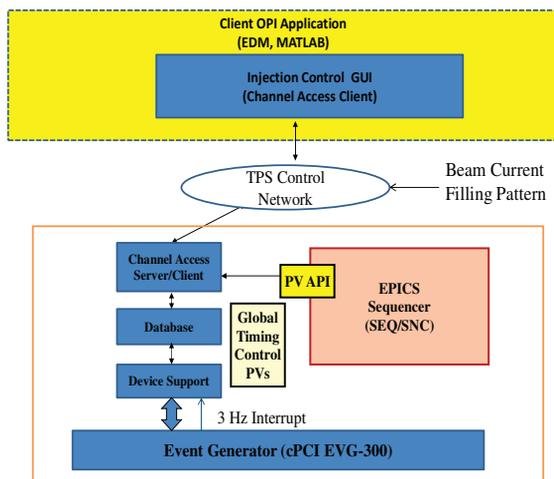

Figure 3: Sequence RAM management: individual trigger event control.

Sequence RAM Programming

The sequence RAM contents can be updated when current cycle stop. The programming can be done within a few msec. It can program cycle-by-cycle at 3 Hz rate easily.

INJECTION CONTROL

Injection control is the main theme of the timing system. Timing events related to the operation of all devices will be defined and associated to a timestamp to specify its happened time. To satisfy individual operation of subsystems and coordinated injection process, various trigger events might need enable and/or disable control. To provide bucket addressing, the timestamp of some trigger events should be adjusted cycle-by-cycle dynamically. The timing sequence is stored at the sequence RAM in the EVG. The EVG plays the timing sequence in 3Hz which is divided from 60Hz AC power system. The RAM stop-interrupt of the EVG is enabled to wake up an EPICS sequencer to re-program the sequence RAM according to the bucket addressing requirement.

Figure 2: Timing sequencer structure.

Sequence RAM Trigger

The sequence RAM will be triggered by the 3 Hz rate which are generated and synchronized with the sync of booster, storage ring revolution frequency and the 60 Hz mains frequency. Trigger at the other repetition rate can be changed if it is necessary. The booster synchrotron will work at 3 Hz rate normally.

Sequence RAM Entry and Timestamp Management

All sequence will be stored at the sequence RAM. There is a timestamp associated each entry. The event can be active when load the desired timestamp. The event can be de-active by replace the event code as NULL event (event code: 0x00), it can active again when the NULL event replace by original event. The timestamp value can be change for budget address requirements. The sequence RAM will be programmed in every cycle. All kinds of the operation can be fulfilled by these mechanisms. The clients can control the timing sequencer to change content in every cycle via pre-defined PVs. The example of sequence RAM management is presented in Fig. 3.
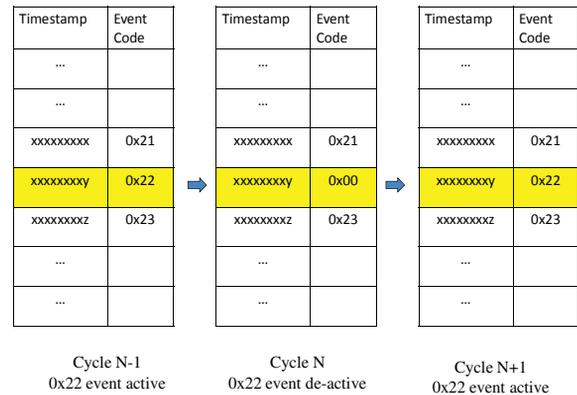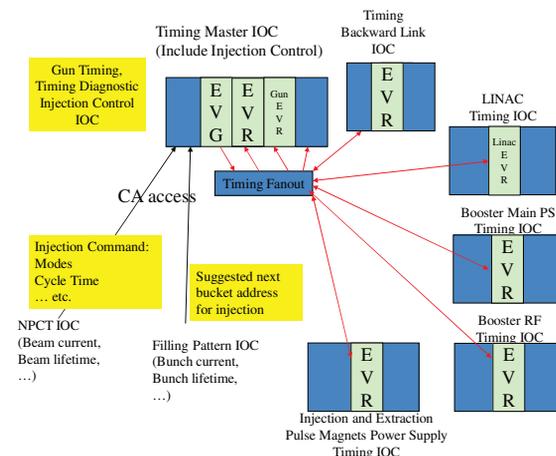

Figure 4: Relationship of injection control related IOCs.

Several IOCs are involved the injection process which are timing master IOC, booster main power supply IOC, booster RF IOC, NPCT IOC, filling pattern IOC, injection and extraction pulse magnets IOC. The relationship of injection control related IOCs is shown in Fig. 4.

The linear accelerator and e-gun triggers will be connected to the timing master and installed at the equipment area (Control Instrument Area, CIA in TPS location name convention) above the linear accelerator system.

Operation Mode

The programmable sequence RAM provides a flexibility to change the operation mode. An EPICS sequencer is implemented to provide the mode control. Basic operation will be ready for commissioning. Sophisticated modes may be delivered later. A simple configuration tool should be available for sequence RAM management. The operation modes may be:

• Individual subsystem trigger enable and disable.
• Single bunch and multi-bunch selection.
• Continuous injection.
• Repetitive rate decimation for specific trigger.
• Warm up trigger for specific device before injection.
• Top-up for desired filling pattern.
• Top-up with filling pattern feedback.

Bucket Addressing

The bucket addressing is performed by changing the value of timestamp in sequence RAM at every cycle. One count corresponds to 8 nsec which is the period of the event clock ($f_{RF}/4$) used by the TPS event system. Bucket addressing scheme is shown in Fig. 5. The cPCI-EVRTG-300 provides the fine delay for gun trigger and digital delay generator for the storage ring injection kicker trigger with 2ns resolution.
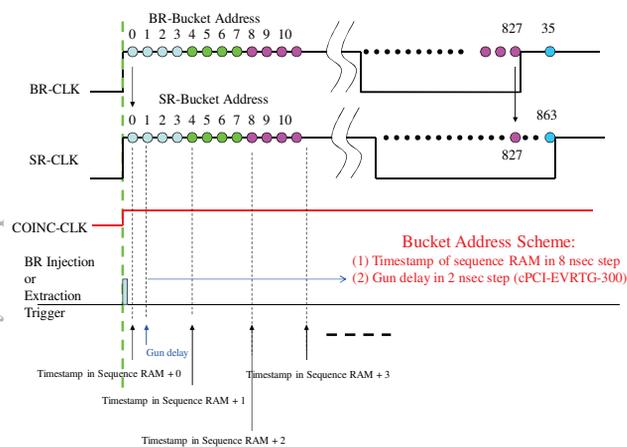

Figure 5: Bucket addressing scheme for TPS

Top-up Injection with Bucket Addressing

The top-up injection scheme might adopt multi-bunch mode to inject beam to desired target current, after reaching the target current the mode is switched into the single bunch mode. According to the filling pattern, the minimum bunch will be filled in next injection.

Filling Pattern Feedback

In order to minimize filling pattern correlated orbit oscillations due to uneven bunch patterns, filling pattern control and/or feedback is planned to minimize bunch-to-bunch variation. Therefore there will be an EPICS sequencer running on the filling pattern IOC that measures bunch structure of storage ring and provides the next injection bucket address to timing master IOC via PV channel access.

Miscellaneous Considerations

Some devices might need a few cycles for warm-up before reaching stable working condition for beam injection, for example the injection septum of the storage ring. This is reported by several light sources. The timing sequencer can program the septum fire one or more cycles before real injection cycle take place. The booster power supplies may be the same. This mechanism may ensure accelerator working in a proper condition before injecting beam.

Implementation

A few timing control related programs are developed by using state notation language (SNL) of the EPICS sequencer. One program waits for the sequence RAM stop interrupt then clears and enables it for next cycle and updates the elapsed time for top-up injection mode. A trigger control program serves the request of trigger on-off of several types of devices which are diagnostic components, injection and extraction pulse magnet power supply, booster synchrotron power supply, Booster RF system, linac system, e-gun and etc that performed by changing event codes in sequence RAM. The main timing control program provides continuous and top-up injection control. The functions have been described above. Another sequence program calculates the injection efficiency and beam lifetime. The beam current of booster and storage ring are averaged by a sequence program running on another IOC which connects booster DCCT and storage ring DCCT. The IOC is located in another CIA. The beam currents are captured as waveforms when the interrupt activated by a Hytec ADC8417 IP module, which is synchronized to the 3Hz time event then averaged with adjustable data points. The EDM page for injection control related programs testing is shown in Fig. 6.

The time difference between consecutive sequence RAM 'stop' interrupts are calculated to evaluate the interrupt response time which includes a kernel driver, asynDriver and pciGeneral[7] device driver (EPICS) of the main timing IOC. The histogram of the response time is shown in Fig 7. Maximum jitter is about 1.5 ms peak-to-peak and the CPU loading of the EPUCS IOC is less than 20%.
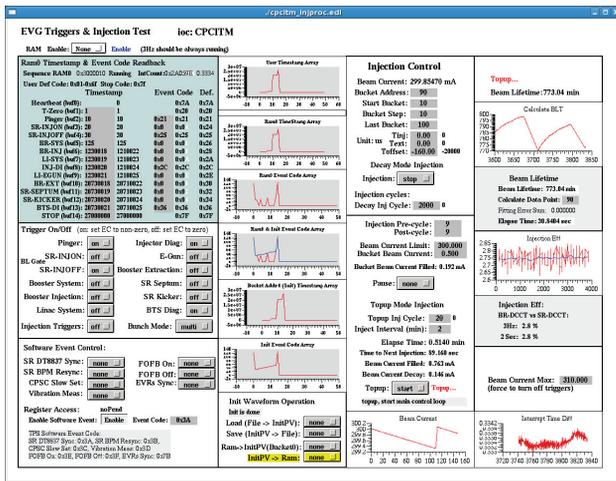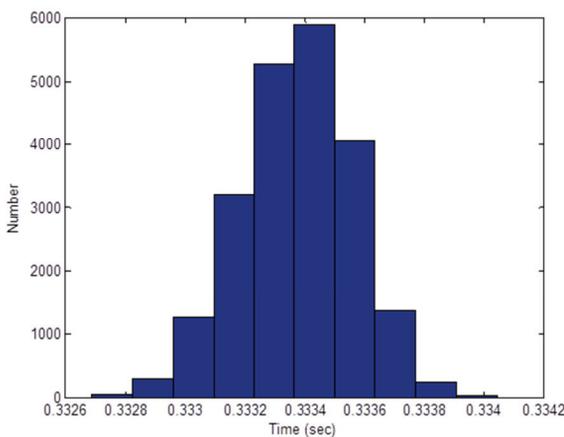
Figure 6: EDM pages for injection control test.

Figure 7: Histogram of time difference between consecutive sequence RAM 'stop' interrupts.

TMING FOR BEAMLINE USERS

Time resolved experiments need machine revolution clock or its sub-harmonics or harmonics to synchronize synchrotron light pulse produced by isolated bunch(s). Event system can provide these functionalities with jitter in 5 ~ 20 psec dependent upon EVR module usage.
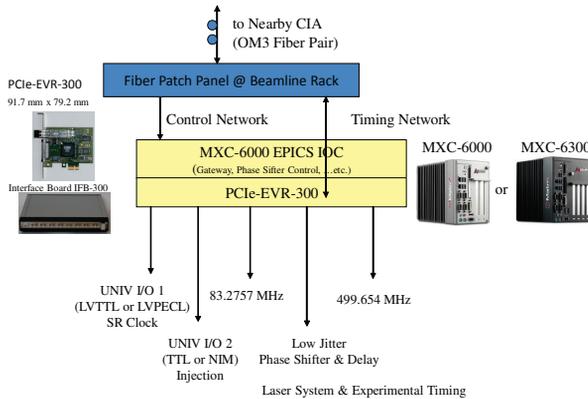

Figure 8: Basic hardware configuration for beamline timing interface in TPS.

The Basic hardware configuration for beamline timing interface in TPS is shown in Fig 8. The latest version firmware allows the distributed bus signal trigger pulse/delay generator and provides a flexible timing option for the experimental stations. Regenerate amplifier clock of the laser system can be generated by this option.

For high precision timing, dedicated RF reference fibre link will send the RF reference to experimental station to re-generate laser clock with jitter in the order of 100 fsec.

CURRENT STATUS

The implementation of the timing system and timing sequencer is ongoing. Various operation scenarios are analysis thoroughly. Prototype test by Matlab scripts was tested in 2011. Change to EPICS sequencer by program using SNL is on-going. Timing fibre network installation will complete in October 2013. Set up of all event system modules equipped EPICS IOCs are scheduled in the first quarter of 2014.

SUMMARY

Implementation of the TPS control system is on-going. Implement various application programs are underway. All components are ready for installation. The timing system will be ready for integrated system test when the TPS installation done.

REFERENCES

[1] C. Y. Wu, et al., "RF Reference Distribution and Timing System for the Taiwan Photon Source", Proceedings of DIPAC2011, TUPD86, Hamburg, Germany.

[2] C. Y. Wu, et al., "Preliminary Testing of the TPS Timing System", Proceedings of IPAC2011, MOPO041, San Sebastian, Spain.

[3] C. Y. Wu, et al., "Timing System for the Taiwan Photon Source", Proceedings of ICALEPCS2011, WEPMS013, Grenoble, France.

[4] C. Y. Wu, et al., "Sequencer Design of Timing System for the Taiwan Photon Source", Proceedings of IPAC2012, WEPPD047, New Orleans, Louisiana, USA.

[5] Micro-Research Finland Oy, "Event Generator", Document: EVG-MRM-0003, 4 January 2011.

[6] Micro-Research Finland Oy, "Event Receiver – Technical Reference", Document: EVR-MRM-003, 7 April 2011.

[7] Jenny Chen, "pciGeneral", EPICS 2011 Spring meeting, http://www.icg.nsrrc.org.tw/EPICS2011