# THE LANSCE TIMING REFERENCE GENERATOR*

R. Merl#, R. Clanton, E. Bjorklund, S. Baily, F. Shelley, LANL, Los Alamos, NM 87545, USA

*Abstract*

The Los Alamos Neutron Science Center is an 800 MeV linear proton accelerator at Los Alamos National Laboratory. For optimum performance, power modulators must be tightly coupled to the phase of the power grid. Downstream at the neutron scattering center there is a competing requirement that rotating choppers follow the changing phase of neutron production in order to remove unwanted energy components from the beam. While their powerful motors are actively accelerated and decelerated to track accelerator timing, they cannot track instantaneous grid phase changes. A new timing reference generator has been designed to couple the accelerator to the power grid through a phase locked loop. This allows some slip between the phase of the grid and the accelerator so that the modulators stay within their timing margins, but the demands on the choppers are relaxed. This new timing reference generator is implemented in 64 bit floating point math in an FPGA. Operators in the control room have real-time network control over the AC zero crossing offset, maximum allowed drift, and slew rate - the parameter that determines how tightly the phase of the accelerator is coupled to the power grid.

## INTRODUCTION

The power modulators at the Los Alamos Neutron Science Center (LANSCE) have gains that change with the phase of the AC power grid [1]. The variation in gain can be up to 30% over the full 360 degree AC cycle. This gain variation is mitigated by forcing the operating point to be phase coupled with AC power. This coupling means that the acceleration of protons, all accelerator timing signals, the timing of protons-on-target, and the subsequent production of neutrons at the Manual Lujan Neutron Scattering Center are all similarly phase coupled to the AC power grid.

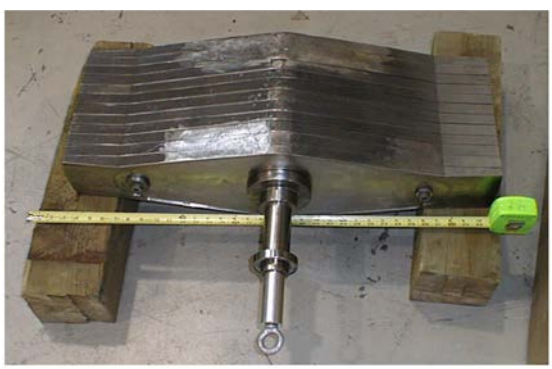

Figure 1: Neutron chopper.

High frequency phase changes can occur on the AC line that are easily tracked by the electronic systems that drive the accelerator timing. All would be well with this situation except for the fact that massive rotating pieces of shielding known as choppers must move into place to block fast neutrons at the neutron scattering center and then rotate out of the way a few milliseconds later. A neutron chopper is shown in Figure 1. These choppers can weigh hundreds of pounds and their motors cannot accelerate and decelerate them fast enough to respond directly to high frequency phase changes in the AC line. If the chopper does not arrive at it's top-dead-center position in time to block the high-energy neutrons, then the distribution of energy at the neutron scattering instruments will not be evenly distributed and the data that instrument collected will have to be discarded. This wastes valuable accelerator beam time and it is something we wish to avoid [2].


Figure 2: The LANSCE timing reference generator.

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#merl@lanl.gov LA-UR-13-26955

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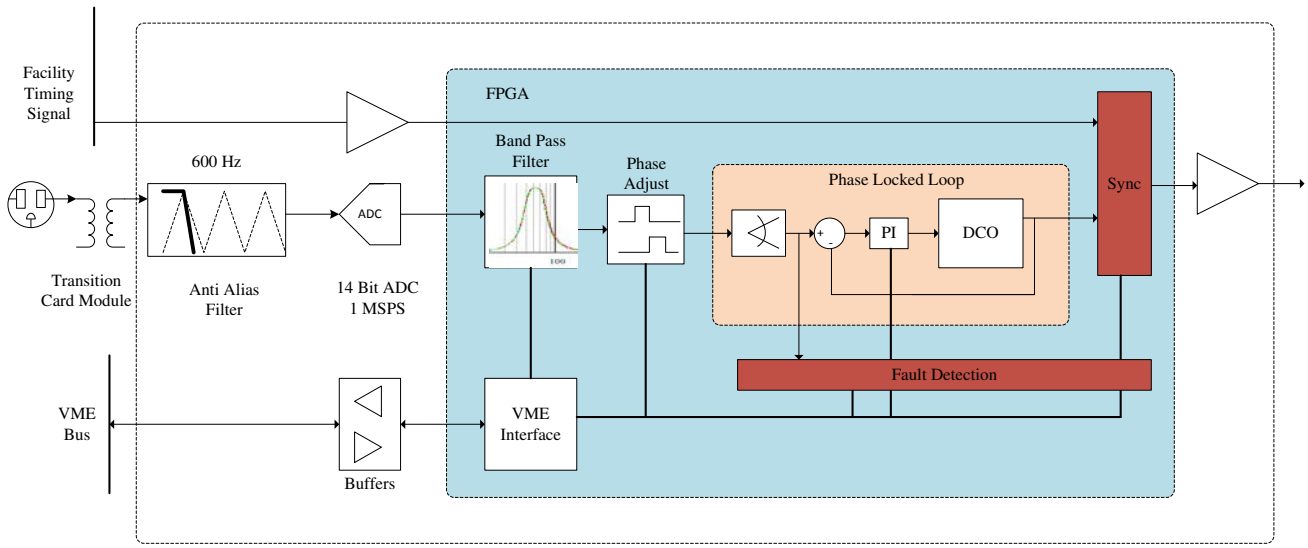


Figure 3: Signal chain diagram.

## THEORY OF OPERATION

Since the operating requirements of the accelerator and the neutron choppers are at odds with each other, a solution was found in a compromise of timing the accelerator to a filtered version of the AC power grid phase. While there can be severe gain variation in the power modulators over the full 8.3 millisecond AC power cycle, allowing the operating point to slip +/- 100 microseconds makes little difference in their performance and can be tolerated. This small slip does allow for a large improvement in chopper performance since the electric motors that drive them have enough bandwidth to track the lower frequency phase changes that remain after this slip in accelerator timing is allowed.

## ARCHITECTURE

An all-digital Phase Locked Loop (PLL) has been developed to couple the LANSCE accelerator to the AC power grid in a way that allows this +/- 100 microsecond slip to occur, but does not allow timing to slip further. This phase locked loop tracks the phase of the power grid, but ignores (does not track) high frequency changes. The PLL smoothes or filters the phase of the raw AC power before it is used by the accelerator timing systems.

### *VME Module*

The PLL has been designed as a 6U VME board to be compatible with and easily integrated into the existing accelerator control system infrastructure. LANSCE relies on the Experimental and Industrial Control System (EPICS) running on 6U VME Input / Output Controllers (IOCs). This board has been designed to easily drop into this system and be controlled remotely from the LANSCE control room through a standard EPICS device driver. A photograph of the VME module appears in Figure 2.

The module has an A16/D16 VME interface with a register map for control and status. Values can be written into the register map for real-time control of the slew rate or natural frequency of the PLL. The interface also offers real time control of the phase angle offset of the PLL. Phase angle control allows control room operators to dial accelerator timing +/- 180 degrees from the zero crossing of the AC power grid. Advanced users may also control the damping of the PLL through the interface. Status bits are returned to the LANSCE control room including the locked status of the PLL and lost or present facility timing signals.

An architectural block diagram of the VME board is shown in Figure 3. An external transformer is used to step the raw 60 Hz AC power signal down to a more manageable 5V AC signal on a VME transition card. That 5V signal is low pass filtered with a six pole low pass Butterworth filter with a 600 Hz cutoff frequency. The low pass filter is used to eliminate digital aliases from the downstream digitized version of this signal.

### *Digitization*

After the anti-alias filter, the analog signal is digitized by a 14-bit Analog to Digital Converter (ADC) at 1 MSPS. The 600 Hz knee in the anti-alias filter is many times lower than the 1 MSPS sample rate of the ADC and easily meets the Nyquist criteria for removing aliased signals. The digital output from the ADC is connected to an Altera Cyclone III Field Programmable Gate Array (FPGA) where the serial data of from the ADC is reassembled into 14-bit fixed point words representing the discrete time values of the AC waveform. At this point in the signal chain, the sample rate of the 60 Hz AC signal is 1 MSPS. This discrete time signal is converted in real time from 14-bit fixed point integer to a 64-bit floating point (double precision) number in the IEEE-754 standard format.

Once the signal is in IEEE-754 floating point format, it can be easily manipulated with Infinite Impulse Response (IIR) structures without suffering from the errors that would be introduced by round off in fixed point implementations. Digital filters and compensators were



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built in VHDL from cascaded second order systems to do the remaining work.

The floating point signal is band pass filtered with a digital four pole filter centered at 60 Hz. This filter removes very high frequency components from the digitized signal as well as any DC offset that may be present earlier in the signal chain.

### *Phase Locked Loop*

The signal is converted from 64-bit to 32-bit (single precision) format and then fed into the digital PLL. The PLL uses a phase comparator to measure the error phase between the PLL output and this input signal. That phase error is operated on by a Proportional – Integral (PI) compensator to generate a correction signal to a Digitally Controlled Oscillator (DCO). The DCO generates the signal used for accelerator timing and is the output of the PLL. The center frequency of the DCO is 120 Hz. The PLL, due to its feedback and PI compensator behaves like a low pass phase filter according to equation (1) [3].

$$G(s) = \frac{\omega_n^2 + 2s\zeta\omega_n}{s^2 + 2\zeta\omega_n s + \omega_n}. \quad (1)$$

Where s is the complex frequency variable, $\omega_n$ is the natural frequency of the loop, and $\zeta$ is the damping factor. The damping factor was set to $1/\sqrt{2}$ for a flat response and the natural frequency is an adjustable parameter that is set by LANSCE control room operators. It's the natural frequency that dictates how tightly the PLL follows its input and in this case how closely the accelerator timing follows the raw AC power grid phase.

Earlier work by L.J. Rybarcyk, et al. [1] showed that a classic PLL with a natural frequency of 0.3 Hz would stay within +/- 100 microseconds of the AC power grid phase and meet the requirements of LANSCE's power modulators. For this reason, this board powers on with a default natural frequency of 0.3 Hz. This value can then be overridden by input from the control room.

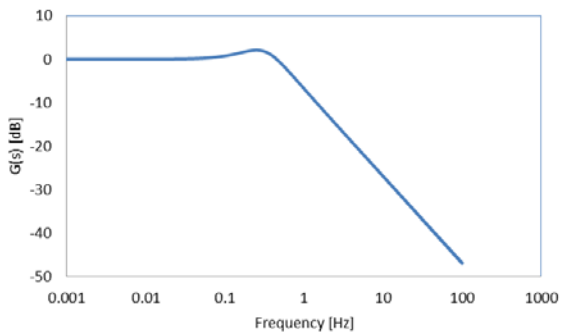


Figure 4: Transfer function for this PLL.

The transfer function for the PLL with the natural frequency set to 0.3 Hz is shown in Figure 4. The transfer function shows that the PLL behaves like a low pass filter for phase signals.

### *Slew Rate*

Accelerator operators at LANSCE can use the EPICS control system to manipulate the slew rate of the timing reference generator in real time. The slew rate has the units of microseconds / machine cycle and is a measure of how much time the reference generator might slew for each machine cycle. It's another way to conceptualize the natural frequency of the PLL. The slew rate as desired by control room operators is converted to natural frequency in the units of radians / second by the EPICS device driver by taking the machine cycle to be approximately 120 Hz.

### *PI Compensator*

The PLL uses a PI compensator to filter the phase error between the DCO and the band-passed instantaneous AC grid phase. The proportional and integral terms of this compensator are what set $\omega_n$, the natural frequency of the PLL. The transfer function, H(s), for a PI compensator is shown in equation (2).

$$H(s) = P + \frac{I}{S}. \quad (2)$$

Equation 2 can be rewritten in terms of $\omega_n$ and $\zeta$ in equation 3, below.

$$H(s) = 2\zeta\omega_n + \frac{\omega_n^2}{S}. \quad (3)$$

Equation 3 can be transformed into the discrete time domain and represented as equation (4).

$$H(z) = \frac{a_0 + a_1 \cdot z^{-1}}{1 - z^{-1}} \quad (4)$$

Where $a_0 = \frac{\omega_n(\omega_n + 2C\zeta)}{C}$ and $a_1 = \frac{\omega_n(\omega_n - 2C\zeta)}{C}$. C is the scaling factor used in the conversion from the continuous time domain (s) to the discrete time domain (z). C = 2 / 8.3 milliseconds. Equation 4 is realized inside the FPGA using the IIR structure shown in Figure 5.

The IIR structure is constructed from multipliers shown with triangles where the signal is multiplied by the coefficient inside the triangle and summed by floating point adders which are shown with circles. The square blocks represent memory registers in the IIR feedback paths and hold their values for one sample period or 8.3 milliseconds.

### *Fault Protection*

In the event that the timing reference generator loses its connection to the raw AC phase reference, the module will continue to output a stream of reference pulses at 120

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Hz with the last known relative phase. If the raw AC phase reference returns, the module will gracefully resynchronize with it without any nonlinear response. During the reference loss and recovery process, the module opens a timing window 100 microseconds wide and centered at the last known reference phase. Reference pulses that fall outside this window are ignored. This window means that the process of recovering takes slightly longer but also rejects noise that can be generated by the zero crossing detector during a loss condition. During any loss of reference, a register bit is set in the module's VME interface that alerts the EPICS control system of the problem. EPICS can then automatically start the process of protecting the accelerator systems by rapidly shutting off the power modulators and other related equipment. Control room operators would also see an indication of the reference loss on their displays. The module has front panel LEDs that can be visually inspected for this condition as well.

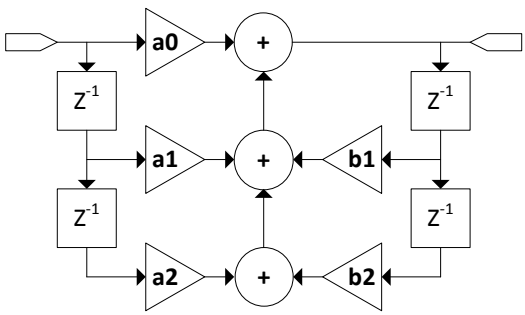


Figure 5: Infinite impulse response structure that implements the PI compensator.

### *Facility Retiming*

The output pulses from the PLL are synchronized with the facility 2.8 MHz timing signal from the LANSCE proton storage ring (PSR). The PSR is downstream from the power modulators and this retiming improves the synchronization between the linear accelerator and the PSR. In the event the 2.8 MHz facility timing signal is lost, the timing reference generator times its subsequent outputs with an internal 2.8 MHz digital oscillator at the last known phase of the 2.8 MHz facility timing signal. This fault condition is reported to EPICS and the control room operators the same way a loss of the AC reference signal would be.

## FUTURE WORK

We look forward to installing this new timing reference generator during the next long accelerator maintenance period and reporting on accelerator performance.

## REFERENCES

[1] L.J. Rybarcyk and F.E. Shelley, Jr., "Improvements to the LANSCE Accelerator Timing System," PAC'97, Vancouver, May 1997, 6P030, p. 2514 (1998); http://www.JACoW.org

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