FPGA IMPLEMENTATION OF A DIGITAL CONSTANT FRACTION FOR FAST TIMING STUDIES IN THE PICOSECOND RANGE

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Abstract

Thermal or cold neutron capture on different fission systems is an excellent method to produce a variety of very neutron-rich nuclei. Since neutrons at these energies bring in the reaction just enough energy to produce fission, the fragments remain neutron-rich due to the negligible neutron evaporation thus allowing detailed nuclear structure studies. In 2012 and 2013 a combination of clover and standard coaxial Ge detectors plus very fast $LaBr_3$ scintillators has been installed at the PF1B cold neutron beam of the Institut Laue-Langevin (ILL). The present paper describes the digital acquisition system used to collect information on all gamma rays emitted by the decaying nuclei. Data have been acquired in a trigger-less mode to preserve a maximum of information for further off-line treatment with a total throughput of about 10 MByte/sec. Special emphasis is devoted to the FPGA implementation of an on-line digital constant fraction algorithm allowing fast timing studies in the pico second range.

INTRODUCTION

Presently a common characteristic trend in low and medium energy nuclear physics is to develop complex detector systems to form multi-detector arrays. The main objective of such an elaborated setup is to obtain comprehensive information about all reaction products. State-of-art γ-ray spectroscopy requires nowadays the use of large arrays of high purity Germanium (HPGe) detectors often coupled with anti-Compton active shielding to anti-gate on escape Compton radiation from the Ge detectors and to reduce the ambient background. Those large arrays are presently often completed with very fast $LaBr_3$(Ce) scintillators to obtain precise timing information on the half-life of nuclear excited states.

In view of the complexity of the signals acquired by the detectors, the front-end electronics must provide precise information about their energy, time and possibly pulse shape. The large multiplicity of the detection system requires the capability to collect the multitude of signals from many detectors, fast processing and very high throughput of more than a million data-words/s. The possibility to handle such a complex system using traditional analogue electronics has shown rapidly its limitation. Nowadays digital pulse processing systems are available with performances close to the corresponding analogue systems. With the modern digitisers the restrictions of the A/D conversion have been reduced because of the increase in sampling frequency and in resolution in terms of the number of bits. Besides the loss of information due to the A/D conversion error, the major problem of the fully digital approach is the huge amount of data to handle. In order to reduce the amount of data to be transferred, a Field Programmable Gate Array (FPGA) can be used to perform on-line digital pulse processing and consequently extract and save only the relevant quantities.

Our specific digital acquisition engine will be discussed in the next sections together with the experimental setup and the results obtained in recent campaigns of measurements.

EXPERIMENTAL SETUP

All the measurements have been performed at the PF1b beam line of the ILL. Neutrons are delivered to the beam position by the H113 ballistic neutron guide [1], characterised by a maximum flux at the wavelength of 4Å of about 2×10^{10} neutrons/cm^2/s on a total beam size of 20 cm $\times$ 12 cm. To match a closer geometry for the detectors, more suited for measurements with low cross section, the beam size has been reduced to a diameter of about 1 cm at the sample position by introducing a series of boron and lithium collimators upstream.

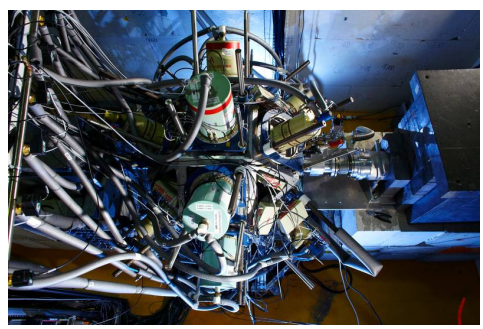

Figure 1: Detectors setup in use for the nuclear spectroscopy experiments.

A simple sample holder capable of keeping the sample in a stable and reproducible position was used for all measurements with stable isotopes, while an evacuated sample chamber was adopted for measurements with fissile materials to ensure an additional physical barrier limiting the risk of environmental contamination in the unfortunate case of damage to the sample itself.

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Detector Arrays

Two different setups have been adopted depending on the main goal of the experiment. To optimise the *gamma*-ray detection efficiency for nuclear spectroscopy measurements we used a detector array containing 16 HPGe detectors and their corresponding active bismuth germanate BGO suppression shields. For the fast timing experiments 8 HPGe detectors have been replaced by 16 $LaBr_3$(Ce) fast scintillators. Those fast response scintillation detectors have, on one hand a good energy resolution of about 3% and, on the other hand an excellent time response. Because of these characteristics they are particularly suited to measure level lifetimes in the range from a few picoseconds to several nanoseconds [2].

Figure 1 depicts the different detectors and their placement in space for the setup in use during the nuclear spectroscopy experiments. Passive heavy metal collimators have been placed in front of the entrance window of the detectors to reduce their background and cross-talk. All the signals from the BGOs were recorded together with those from the HPGe and $LaBr_3$(Ce) and the anti-coincidence discrimination has been performed off-line to prevent any undesired loss of data.

DIGITAL ACQUISITION

Depending on the specific detector setup, the data acquisition system was handling from 68 (spectroscopy) to 72 (fast timing) separate channels. The analogue signals from the detector preamplifiers were sampled by 10 V1724, 8 channels 14 bit 100 MS/s CAEN digitiser [3]. The numerical information about the amplitude of the analogue signals and their arrival time were collected by two RIO3 PowerPC-based VME single board computer [4] (data concentrator) before being recorded on a computer hard disk.

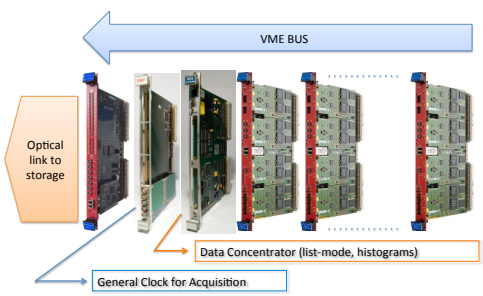

Figure 2: Layout of the digital acquisition chain.

Figure 2 shows the of the digital acquisition system that was adopted for on the experiment. The total achieved event rate was of about 900 kHz events corresponding to a data rate of 7.2 MByte/s. In the following sections more exhaustive details on the algorithm used by the digitisers and on the data concentrator cards are given.

Pulse Processing Algorithm

The purpose of the Digital Pulse Processing (DPP) is to perform on-line signal treatment able to transform the row sequence of samples into a compressed data format that preserves the relevant information. For this purpose, a specific algorithm implemented in the FPGA which equipped each channel of the digitisers allows to extract the amplitude and/or the arrival time of the detected pulses. The pulse conversion starts as soon as a trigger is generated. In our case, this happens via a voltage step overtaking a programmable digital threshold rather than comparing the absolute voltage level, as in the case of analogue systems. For an accurate time determination, the traditional approach would make use of a Constant Fraction Discriminator (CFD), where the zero crossing of the sum of the input and the delayed, attenuated and inverted input, delivers the desired information independently from the amplitude of the pulse. In our case, the FPGA calculates the second derivative of the input signal (the direct output of the detector preamplifier). The input signal can be represented as the sum of two exponential decays being the fast component determined by the time constant of the detector and the slow one by the RC of the preamplifier. A simple calculation demonstrates that the zero crossing of such a second derivate depends only on the two time constants while it does not depend on the pulse amplitude. The zero crossing of the second derivate of the input signal delivers, therefore, an accurate time determination with an uncertainty equivalent to one unit of the sampling time.

A trapezoidal filter is applied to the input signal to transform the typical exponential decay generated by a charge sensitive preamplifier into a trapezoid [5]. The height difference between the signal baseline and the flat top of the trapezoid is proportional to the amplitude of the initial pulse. This trapezoid plays more or less the same role of the shaping amplifier in a traditional analogue acquisition system. We want to highlight the analogy between the two systems: both have a shaping time constant and must be calibrated for the pole-zero cancellation. For both, a long shaping time gives a better energy resolution but increases the probability of pile-up. Both are AC coupled with respect to the output of the preamplifier whose baseline is hence removed, but both have their own output DC offset, which constitutes another baseline for the peak detection. Setting the parameters of the trapezoidal filter is equivalent to changing the shaping time in a classical spectroscopy amplifier.

Digitisers

The model used is the CAEN waveform digitiser board V1724. It is a 1-unit wide VME 6U module housing 8 channels 14 bit 100 MS/s flash ADC with threshold auto-trigger capabilities. Trigger signals can be provided via the front panel input as well as via the VME bus, but they can also be generated internally, as soon as a programmable voltage threshold is reached. The individual auto-trigger

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of one channel can be propagated to the other channels and onto the front panel trigger output. The board features a front panel clock/reference I/O and a PLL circuit for clock synthesis from internal/external references. In this way, several boards can be phase locked to an external clock source or to a V1724 master clock board. The digitisers consist of a common motherboard housing specific mezzanine cards for each channel. The motherboard houses the clock logic management and the readout control FPGA that provides the trigger management and acts as a bridge between the local bus and the different interfaces (VME 64X, Optical link, PCI express, USB 2.0). Mezzanine cards house the input front-ends and the channel FPGA that accounts for the analog-to-digital conversion, the digital pulse processing algorithm and the memory buffers. The readout control FPGA accesses the mezzanine cards through the local bus.

Data Concentrator

The real-time acquisition engine is implemented in a Power PC based VME board computer equipped with 256 MB of memory. This board does not contain any operating system to optimise real-time performances and to prevent any dead time. A specific set of routines has been developed to implement all the functionalities necessary to configure and access the digitisers. The real-time processing algorithm running in the processor is able to handle total event rates of more than 1 MHz, providing on-line display for singles and coincidence events of multiplicity 2. The primary purposes of the data concentrator card is to create the data structures containing the variables and the parameters for the acquisition. Once the digitisers have been initialised and programmed, the concentrator is reading the data by emptying the digitiser's buffers using MBLT transfer mode over the VME bus. Each event is then on one hand analysed to produce the relevant real-time histograms and, on the other hand, stored in a double buffer memory once all the information necessary to define a list-mode event have been added. The instrument control software (see next section) is then reading asynchronously the card's memory, via a PCI optical link, to transfer the list-mode events to the external mass storage and to display the histograms.

Control Software

The instrument control software is acting as interface between the acquisition hardware and the user. It offers a full graphical interface to access all parameters related to the configuration of the digitisers as well as of the acquisition card. It allows real-time visualisation of all relevant spectra including single and multiplicity 2 events. The software integrates an oscilloscope mode display used during the setup phase to tune the sampling parameters for each channel of the digitiser cards. This mode offers the unique advantage to visualise instantaneously the effects of any parameter modification with respect to all signals involved in the acquisition. With our new fully digital acquisition system we could achieve an average resolution for all Ge crystals of about 2.4 keV at 1408 keV γ line from ^{152}Eu source. For $LaBr_3$(Ce) detectors we obtained an average slightly better than 3% at 1408 keV, result which is consistent with what can be obtained with an equivalent analogue system.

DIGITAL CONSTANT FRACTION DISCRIMINATOR

The design of an on-line digital constant fraction discriminator (CFD) is stimulated by the ability to produce a very accurate pulse-time information. This signal, in the ideal case, is precisely related in time to the occurrence of an event eliminating the amplitude-dependent time walk. In order to provide an alternative to the standard analog approach based on time-to-amplitude converters (TAC) we have developed and tested during the second half of the EXILL campaign, a new real-time CFD system.

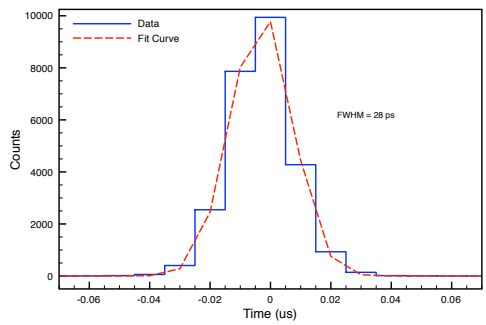

Figure 3: Time dispersion obtained using a pulse generator sending the same pulse on 2 different digitiser channel.

The goal was to maintain the excellent performances of the TAC, capable of time resolution of a few tens of picoseconds. Our design has been fully implemented in hardware and does not add any dead-time to the acquisition chain. The system consists of two main elements: a number of digitisers according to the required number of channels and a digital-CFD card providing real-time CFD algorithms for timing accuracy. The analog signal from the $LaBr_3$(Ce) scintillators was digitised by a CAEN flash ADC waveform digitiser, model V1751. This model is a 1-unit wide VME 6U module housing a 8 channel 10 bit 1 GS/s flash ADC with threshold auto-trigger capabilities. Thanks to several memory buffers for the triggers and the samples, subsequent acquisition windows can be stored without any dead time between them. Therefore, the acquisition can take place without the loss of any event, no matter what is the frequency and the distribution of them, at least until the readout rate allows the emptying of the memory.

Each channel has a SRAM memory buffer, with independent read-write access divided in 1 to 1024 buffers of programmable size. The board houses a daisy-chain optical link able to transfer data at 80 MB/s. The digital-CFD board consists on a VME64X configurable high den-

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sity I/O connection carrier board based on the latest Xilinx Virtex-6T FPGA. The internal architecture of the FPGA is designed as a Network on Chip (NoC) approach including 1 GB DDR3 shared memory controller with IDMA. The board is the result of a common development between the company IoXoS in Switzerland and the ILL. Using the board edge to edge interconnection solution which provides full PCB front end area utilisation, we are able to communicate with the optical link of the digitisers using the CAEN proprietary protocol CONET2 and to readout the data stored in the circular buffers of the flash ADC at very high event rates. The main purpose of the digital-CFD board is to perform on-line a specific CFD algorithm on the sampled pulse-shape to obtain an accurate timing in the ps range. In such a way, only the digitiser's time-stamp and the calculated event arrival time will be stored in the list-mode data flow reducing considerably the amount of recorded data. Figure 3 shows the results obtained using a pulse generator producing pulses with timing similar to those produced by a $LaBr_3$(Ce) scintillator, e.g. 20 ns rise-time and 200 ns decay-time. By sending the same pulse on 2 different channels one can evaluate the intrinsic time resolution achievable with the adopted electronics and algorithm. After tuning the parameters of the CFD algorithm we obtained a dispersion of 28 ps.

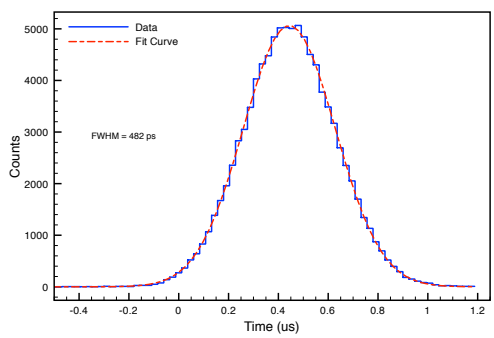

Figure 4: Time dispersion obtained with two $LaBr_3$(Ce) detectors placed in front of a ^{22}Na source.

The second part of the test has been performed using a ^{22}Na radioactive source placed in between 2 $LaBr_3$(Ce) detectors. An energy window centred around the 511 keV annihilation lines has been used to select the relevant events from the background to avoid random coincidences. Because of the prompt γ emission ($\Delta t < 1$ ps) the broadening of the obtained time distribution (see Fig. 4) represent a direct measure of the intrinsic time resolution of the setup. This includes the detector assembly rise-time (crystal plus photomultiplier) and the uncertainties introduced by the finite sampling and the fitting procedure as evaluated in the measurement with the pulse generator. A total time dispersion of less then 500 ps has been obtained. A full characterisation of the detector setup and of the total achievable performances is still ongoing.

CONCLUSION

The campaign of measurements have been supported by 80 different scientific proposals for a total beam time request of 100 days. The experiment has been a great success and only less then 5% of the beam time has been lost due to technical problems or configuration change over. A total of 24 different samples have been irradiated in a neutron beam of 10^8 n/cm^2/s, including ^{235}U and ^{241}Pu samples. Two different setups have been used for spectroscopy and fast timing measurements consisting up to 50 Ge crystals and 16 $LaBr_3$(Ce) fast scintillators operating simultaneously. A fully digital, trigger-less, acquisition system has been developed and it has proven to be able to handle considerable event rates up to almost 1 MHz. A total amount of about 60 TB of data has been produced and stored in a grid-based distributed system (IRODS) allowing a user friendly access to the data. The potential of the trigger-less data has been proven since no a priori condition has been imposed to the data collection leaving total gating freedom in the off-line analysis. From the more technical point of view, the development of a new digital constant fraction has been pushed forward profiting of the presence on site of very good quality $LaBr_3$(Ce) scintillators for the testing phase.

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