ELECTRONICS DEVELOPMENTS FOR HIGH SPEED DATA THROUGHPUT AND PROCESSING*

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Abstract

The European XFEL DAQ system has to acquire and process data in short bursts every 100 ms. Bursts lasts for 600 µs and contain a maximum of 2700 X-ray pulses with a repetition rate of 4.5 MHz and detector data captured has to be processed before the next burst starts. This time structure defines the boundary conditions for almost all diagnostic and detector related DAQ electronics required and currently being developed for start of operation in 2016. Standards used in the electronics developments are: MicroTCA.4 and AdvancedTCA crates, use of FPGAs for data processing, transfer to backend systems via 10 Gbps (SFP+) links, and feedback information transfer using 3.125 Gbps (SFP) links. Electronics being developed in house or in collaboration with external institutes and companies include: a Train Builder ATCA blade for assembling and processing data of large-area image detectors, a VETO MTCA.4 development for evaluating pulse information and distributing a trigger decision to detector front-end ASICs and FPGAs with low-latency, a MTCA.4 digitizer module, interface boards for timing and similar synchronization information, etc.

INTRODUCTION

Construction of the European X-Ray Free-Electron Laser facility (European XFEL) started in 2009 in Hamburg, Germany. From 2016 on, European XFEL will generate intense, ultra short coherent X-ray flashes for scientific applications. The project is one of the first ESFRI projects [1] to be implemented, 12 European states contribute to the project.

The electron accelerator used to generate X-ray flashes is a further development of the superconducting technology used by FLASH at DESY. The balance between cooling capacity and heat generated in the RF accelerating cavities allows electron bunches generated at 4.5 MHz to be accelerated to 17.5 GeV for 600 µs every 100 ms. The non-continuous delivery of trains of pulses, see Figure 1, is a major challenge to detector and DAQ designers.

In this paper DAQ and control electronics developed to facilitate acquisition and on-the-fly processing on high data throughput imaging, digitizer and other detectors used in experiments is described.

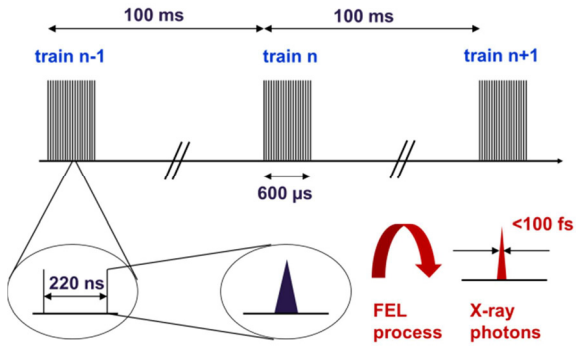

Figure 1: Beam delivery time structure.

DAQ AND CONTROL INTERFACES

The architecture of the European XFEL data acquisition system [2] foresees five layers: detector front end electronics, front end interfaces, PC farm layer, data cache and computing clusters, and offline data archiving and computing clusters. The use of layers with well-defined interfaces allows for scalability and flexibility, by extension of layer resources and introduction of additional layers, respectively.

Interfaces

Front end electronics designed for use at the facility must comply with the DAQ and control interfacing standards used:

- Control – 100 Mbps or 1 Gbps Ethernet (RJ45, TCP)
- DAQ – 10 Gbps Ethernet (SFP+, TCP or UDP)
- Feedback – 3.125 Gbps (SFP, custom)
- Synchronization and tagging – PCIe or serial lines

Timing System Interface

The timing system developed by the electron machine control group delivers synchronization signals, clocks and beam related metadata (unique train number, train pulse pattern identifier, etc.) used for tagging to the front end systems via a custom MTCA.4 Timing Receiver board [3].

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IMPLEMENTATION BASELINES

Development of electronics for use in the photon beam lines and experiments has benefit greatly from use of the following design and implementation standards:

- MTCA.4 or ATCA crates are used for DAQ developments
- XiLinx FPGAs and IDE are used

DUAL 10GBPS IO FMC MEZZANINE

The dual 10 Gbps IO FMC mezzanine has been developed by DESY [4] for use with Train Builder, see below, and large 2D imaging detector [5,6,7] front end systems at the European XFEL. The board has become a baseline feature of many systems including non-project related developments. When development started in 2009 10 Gbps Ethernet was emerging as a commercially attractive high performance link standard whose transfer rate matched those required for 2D camera modules and single channel digitizers to be operated at the European XFEL.

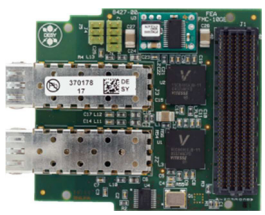

Figure 2: Dual 10 Gbps FMC mezzanine [4].

The FMC mezzanine connects via an ANSI/VITA57 standard high density FMC connector to the motherboard. Eight FPGA GigaLink Transceiver Ports operating at 3.125 Gbit/s are grouped into two independent XAUI interfaces to implement two 10G channels. These are feed into a physical interface PHY, VSC8486 from VITESSE, on the FMC which performs the conversion from XAUI (10B/8B) to XFI (10 Gbps 64B/66B serial) for use by an optical or copper SFP+ transceiver. The VSC8486 supports directly the SFP+ interface, has a single supply voltage of 1.2 V, low power consumption of 0.75 W, several loopback modes and other useful error correction features. Firmware modules implementing UDP are used.

A large number of FMC are in use and the solution will remain attractive, progress, however, does not stop and the ability of the Vertex-6 and later FPGA versions to drive directly the SFP+ transceiver means that later developments, including the digitizer described later, do not require the FMC.

TRAIN BUILDER ATCA BOARD

The Train Builder demonstrator [8] is an Advanced Telecom ATCA data acquisition board being developed by STFC Rutherford Appleton Laboratory for the European XFEL. The board is primarily designed to provide a common off detector readout system for the large 2D pixel detectors being developed for use at the facility. Each 2D detector has one Megapixel sensor elements subdivided into 16 regions or modules. These are read out off-detector using optical data links each operating at 10 Gbps. Each link produces up to 512 partial X-ray images (from their respective sub-region) during each train of X-ray pulses. The train repetition rate of 10 Hz results in a total data rate per detector of up to 10 GBytes/sec. Detector data is received by the Train Builder system located up to 100m from the detector. The Train Builder exploits the regular time structure of the facility and uses a time switched multiplexing architecture to build data from input modules into complete Megapixel images which are sent on to the PC-layer. Key elements of the design are: processing units, deep memory buffers, a switching device and 10 Gbps IO links.

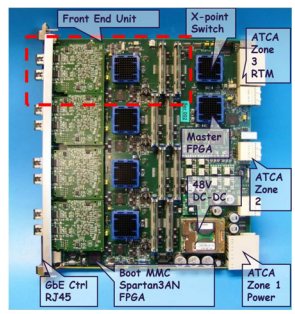

Figure 3: Train Builder ATCA board [8].

The demonstrator board has been developed, Figure 3, in standard 8U x 280 mm ATCA form factor card to validate the design. At the front of the board are four copies of a Front End unit circuitry each with an ANSI/VITA57 standard high density FMC connector, which are equipped with the dual 10 Gbps SFP+ FMC mezzanine cards described above. Each FMC is connected to the main I/O and processing engine, a Xilinx Virtex-5 FPGA (FX100T), via 8 Multi-Gigabit Transceiver (MGT) lanes (4 TX&RX lanes per 10G link). The data links are all fully bi-directional.

Each Virtex-5 is connected to a pair of independent DDR2 VLP SODIMM (very low profile modules to meet ATCA board mechanical specifications) with each SODIMM providing up to 2 GBytes of data buffering. The Virtex-5 devices contain dual PowerPC440 embedded processor cores which manage the DDR2 memory controller DMA engines. Each FPGA has an SRAM to store the software for both embedded processors. In addition each Virtex-5 is equipped with a QDRII external memory (2Mx36b). This fast static RAM, with independent read and write channels, permits full speed manipulation of small chunks of data and is used for the reordering of pixels within an image. This is in contrast to the DDR2 which provide deep buffering and are optimised for fast storage of long streams of consecutive addresses.

The remaining 8 MGT lanes on each FPGA are all connected to a central analogue crosspoint switch (80x80) (Mindspeed M21145). The crosspoint is also wired over 32 MGT lanes to connectors on the ATCA Zone 3 (Rear Transition Module, RTM, zone). It can be dynamically

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programmed to connect any MGT lane on any FPGA to any neighbour and/or to the Zone 3 with a switching time of a few microseconds. The switch is protocol agnostic and is operated as a simple barrel shifter. In normal operation MGT lanes will operate at up to 3.125 Gbps, however, the switch can run at up to 6.5 Gbps. All MGT links can be configured to operate either using the local 156 MHz clock from each FMC or from a common 156 MHz crystal on the TrainBuilder motherboard.

The symmetry of the board connectivity means that any of the I/O FPGAs can be configured either as a receiver from a detector link or as a transmitter to a PC. Larger systems can therefore be built up using only one version of the ATCA board.

A separate Master Virtex-5 FPGA controls the crosspoint switching and synchronises the I/O FPGAs. An external PHY connects the Master FPGA to an electrical GbE link on the front panel for PC control. The Master is also connected via the ATCA Zone 2 by PCIexpress fabric and the GbE base channels for communications with an optional ATCA hub card.

A small Xilinx Spartan3 (3S400AN) FPGA (with embedded Flash memory) provides limited Module Management Controller functions for the standard ATCA Zone 1 power. It is estimated that the board will dissipate up to 150 W when fully operational. It also monitors temperature sensors which are provided to shut down the board power in the event of a system cooling failure. The VLP SODIMMs have been oriented to allow a smooth air flow over the board. A system ACE controller and associated Compact Flash card provide configuration storage for the Virtex5 FPGA bit files and associated embedded software files. All digital components are located on a dedicated JTAG chain for Boundary Scan.

The first demonstrator boards manufactured in early 2012, passed all basic functionality tests and are being used for FPGA firmware development and throughput and on-the-fly data processing test and development. The targeted ~1 GByte/s on each IO channel has been achieved and initial results concerning QDRII reorganization of input pixel data into row major ordering are promising.

Quarter Mpx detectors will be ready for testing in 2014, their DAQ requirements can be satisfied by a single demonstrator board. Initial tests of connecting two demonstrator boards via Zone 3 cabling producing a ½ Mpx readout system have been made. To achieve 1 Mpx systems the baseline proposal is to connect demonstrator boards via an additional large switch implemented on a board derived from the demonstrator.

LARGE 2D DETECTOR SYNCHRONIZER

A clock, control and VETO synchronization MTCA.4 system [9] has been developed by UCL for the European XFEL as a common interface to large 2D detector front end modules. The system consists of a front side digital board, currently a DAMC2 [10], and a RTM connected via the upper, non-backplane, 60pin ADF connector. The DAMC2 Vertex-5 FPGA interfaces p2p clock and trigger events, and bussed tagging information telegram signals distributed by an in-crate Timing Receiver board. Interfacing to the VETO system, see below, is via the DAMC2 front panel SFP connector. Driven through 54 differential links the RTM distributes to up to 16 detector Front End Modules (FEM) using a TYCO RJ45 plug battery. Signals transmitted are:

- an uninterrupted stable 99 MHz clock derived from the timing system or generated on the RTM PLL for standalone operation.
- Serialized at the clock frequency: train start, stop and reset triggers, and train number and bunch pattern identifier metadata.
- Serialized VETO decisions phase aligned with the bunch frequency

A FEM status message is received from the FEM. The system is extendable to 6Mpx by adding 5 additional slave DAMC2-RTM units.

MTCA.4 DIGITIZER

Many detectors (APD, TOF, delay line, etc.) in use at synchrotron and free-electron laser facilities require digitization of sensor signal. The European XFEL electronics group in collaboration with SP-Devices [11] implemented the first commercially available MTCA.4 digitizer system and provided baseline digitizers for use at the facility.

The development strategy taken was to extend the modular approach already used by SP-Devices to support different commercial buses (e.g. cPCI1/PXIe and PCIe) where a mother board (ADQDSP) supporting the baseline functional requirements (Vertex-6, IO, etc.) of the appropriate bus form factor is used to host ADC mezzanine boards. A consequence of this approach is that the entire family of digitizer implemented (2 – 8 GS/s, 14 – 8 bit resolution) become immediately available to the user. The physical implementation required applying the smaller ADQDSP PXIe layout design to the larger MTCA.4 board and using the remaining real-estate to implement the missing DAQ and feedback interfaces and AMC connector. The control interface is currently provided by the crate host.

First series manufactured board have been available since spring 2013, see Figure 4. These are currently undergoing end-to-end field tests in experiments at the PETRA3 synchrotron radiation facility.

Figure 4: MTCA.4 SP-Devices digitizer [10].

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Identifying and eventually integrating and using higher performance (≥ 20 GS/s) digitizers remains a task to be done.

FRONT END VETO SYSTEM

The DAQ and control interfaces foresee a feedback connection to interconnect FPGAs. A VETO trigger system is being implemented which will use the feedback interface channel to distribute a keep/reject decision for individual images acquired by front end systems during train delivery. This is particularly important for the large 2D detectors being developed which have limited analogue or digital pipeline storage capacities, where a reject decision will free a storage cell for reuse by a later pulse within the same train.

The VETO system implementation consists of three distinct units: sources, an evaluation unit and sinks. Sources are detector systems (e.g. APD, 1D strip detectors, etc.) which can quickly, typically within a few tens on micro-secs, send quality of detected pulse signal to a central clause evaluation unit. The latter evaluates information for all sources and distributes the result to all sink components connected. On receiving a reject decision the sink detector front end system frees resources associated with the pulse for reuse. All detectors conforming to the DAQ and control interfacing standard are capable of participating in the VETO, thus no new source or sink hardware is required. The central clause evaluation unit will use existing MTCA.4 digital boards. Information transferred within the VETO use a custom low latency protocol to minimize FPGA to FPGA transfer times.

EXTERNAL TIMING ADAPTER

The ETA, see Figure 5, is an adapter board, packaged in a small box, used to distribute synchronization triggers, clocks, serialized metadata, and 5V power to systems which cannot directly use MTCA.4 Timing Receiver because of distance or level shifting requirements. Targeted systems are: GigE diagnostic cameras (trigger), Beckhoff PLCs (tagging metadata), and detectors (trigger, clock and metadata) without MTCA.4 interfacing to the DAQ and control system.

Figure 5: External Timing Adapter.

The adapter connects to a RJ45 connector on the Timing Receiver board. The latter supplies 5 V and three freely configurable trigger, clock, or serial metadata which are distributed by the ETA on 4 coax lines. LVDS signals are driven to the adapter using Cat7 cable (≤ 50 m), these are passed to the end user using TTL signals (≤ 5m).

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