DEVELOPMENT OF MICROTCA-BASED IMAGE PROCESSING SYSTEM AT SPRING-8

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Abstract

We have developed a new image processing system based on the MicroTCA platform, which has an advantage over PC in robustness and scalability due to its hot-swappable modular architecture. In order to reduce development cost and time, the new system is built with commercial off-the-shelf products including a Camera Link FMC and a user-configurable Spartan6 AMC with an FMC slot. The Camera Link FPGA IP core is newly developed in compliance with the AMBA AXI4 open bus to enhance reusability. The MicroTCA system will be first applied to upgrade of the two-dimensional synchrotron radiation interferometer [1] operating at the SPring-8 storage ring. The sizes and tilt angle of a transverse electron beam profile with an elliptical Gaussian distribution are extracted from an observed 2D-interferogram. A dedicated processor AMC that communicates with the primary processor AMC via backplane is added for fast 2D fitting calculation to achieve real-time beam profile monitoring during the storage ring operation.

INTRODUCTION

In SPring-8, various charged-coupled device (CCD) cameras have been utilized for electron beam diagnostics of accelerators and X-ray imaging experiments. PC-based image processing systems using PCI capture cards are mainly utilized for the CCD cameras with the Camera Link interface [2]. However, as this is a front-end computer deployed around the accelerators and beamlines, we are concerned about low reliability and the lack of sufficient amount of PCI slots. There are disadvantages such as large footprint and poor maintainability. Furthermore, it is difficult to realize distributed processing by multiple CPU modules through a fast bus.

As a more reliable, flexible and compact solution than a PC, we have developed a new image processing system based on the Micro Telecommunications Computing Architecture (MicroTCA) platform.

MICROTCA

The MicroTCA standard [3] was introduced as a new computing platform for telecommunications and industry. It is a switch-based platform with a high-speed serial interface. The platform has the following advantages in comparison with a PC.

- Modular structure: It provides high scalability owing to its modular structure. Depending on the system scale, we can easily insert advanced mezzanine cards (AMCs) such as FPGA AMCs, various interface AMCs, and so on. A multi-CPU configuration is also available by adding processor AMCs.
- High-speed serial link: It supplies 4 lanes of high-speed serial link called “fat pipe” for each AMC slot. The fat pipe can be selected as PCI Express, 10-gigabit attachment unit interface (XAUI), and serial rapid input/output (sRIO) as the protocol.
- Switch-based platform: The *N*-to-*N* communication between AMCs through the switch module called the MicroTCA Carrier Hub (MCH) is available without reducing the bandwidth of the high-speed serial link.
- Hot swap: Modules can be inserted and removed without turning off power.
- Front access: Module insertion into and removal from the chassis is easy. We do not need to remove the MicroTCA chassis from the 19" rack as with a PC.
- Chassis management: Management capabilities such as power, cooling fan, and thermal management are substantial.

From these advantages, the MicroTCA is expected to be one of the key candidates for the next generation of front-end computers.

IMAGE PROCESSING SYSTEM

We have developed an image processing system using the Camera Link standard to achieve real-time triggering and high-speed data transfer. The MicroTCA Camera Link system for base configuration cameras is made available. Figure 1 shows a photo of our newly developed system.

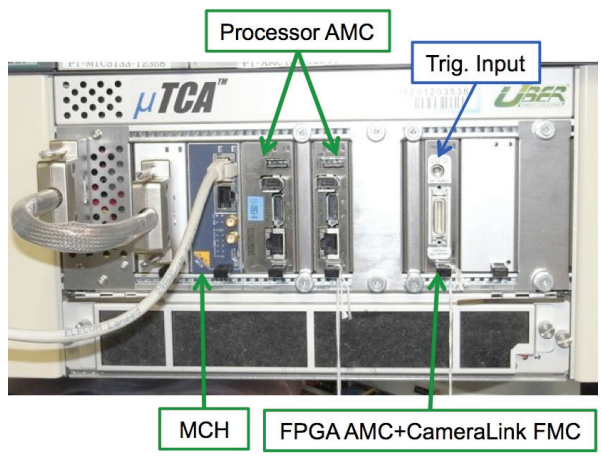

Figure 1: Photograph of MicroTCA-based image processing system.

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Device Components

The new system is built with commercial off-the-shelf (COTS) products to reduce development cost and time. In FPGA development, we employed the FPGA mezzanine card (FMC) standard [4] to enhance the input/output flexibility in a wide variety of applications. A Camera Link base configuration FMC (ARKUS Axfmc0100) and user-configurable Spartan6 FPGA AMC with an FMC slot (TEWS TAMC631) were selected. In order to enhance the reusability of FPGA IP core, we utilized the Advance Microcontroller Bus Architecture (AMBA) Advanced eXtensible Interface 4 (AXI4) [5] to connect the newly developed FPGA function blocks.

By using the high-speed backplane of the MicroTCA, we designed the system to realize distributed processing by multiple-processor AMCs. We are also considering a configuration to handle many Camera Link interfaces in a single processor AMC. The captured image from the Camera Link interface is transmitted to the processor AMC by PCI Express x1 via the MCH. A new Linux device driver and library have been developed for the Spartan6 FPGA AMC comprising the Camera Link FMC.

The device components used in the new system are listed in Table 1.

Table 1: Device Component

MicroTCA Chassis	6Slot Type (UBER)
MCH	PCI Express x4 (NAT-MCH)
Processor AMC	4-core 2.1GHz Core i7 (AM312) 2-core 2.2GHz Core i7 (AM310)
FPGA AMC	Spartan6 LX150, PCI Express x1 with an FMC slot (TAMC631)
Camera Link FMC	Base Configuration (Axfmc0010)

Camera Link IP Core

We have developed the Camera Link FPGA IP core for a combination of Camera Link FMC and FPGA AMC with FMC slot (Figure 2). The newly developed FPGA IP

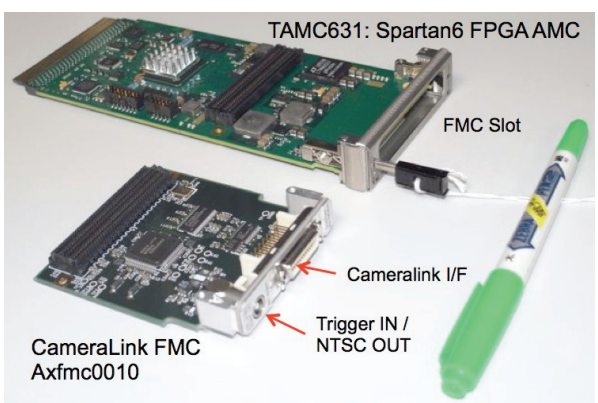

Figure 2: Spartan6 FPGA AMC with FMC slot and Camera Link FMC.

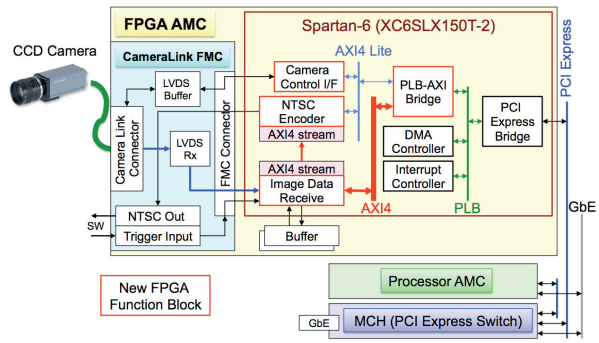

Figure 3: FPGA block diagram.

consists of the camera control interface block, image data receive block, NTSC encoder block, and PLB-AXI bridge block, and they are connected to the AXI4 open bus. We have completed the Camera Link FPGA IP core by combining these newly developed functional blocks and the manufacturer-provided blocks, such as a DMA controller, interrupt controller, and PCI Express bridge. Figure 3 shows the FPGA block diagram.

The data are first acquired via the Camera Link FMC and buffered in a DDR3 memory on the FPGA AMC. Using the double buffer on the DDR3 memory, we assigned alternating writing and reading areas for image data. The FPGA AMC is connected with the processor AMC by PCI Express x1 via the MCH. The image data are transmitted from the reading area of double buffer to a receive buffer in the DDR3 DRAM on the processor AMC by using DMA. In order to support a wide variety of CCD cameras, the various Camera Link parameters are modifiable by the registry settings. We also implemented an external trigger function, trigger counting function, and frame counting function to ensure synchronized image acquisition.

Linux Driver and Library

We have selected the CentOS 6.3 to be compatible with the Red Hat Enterprise Linux 6 for which the TAMC631 manufacturer supports the device driver. The camera control function is added to the TAMC631 Linux device driver. In order to realize parallel processing from multiple applications, we built a ring buffer in shared

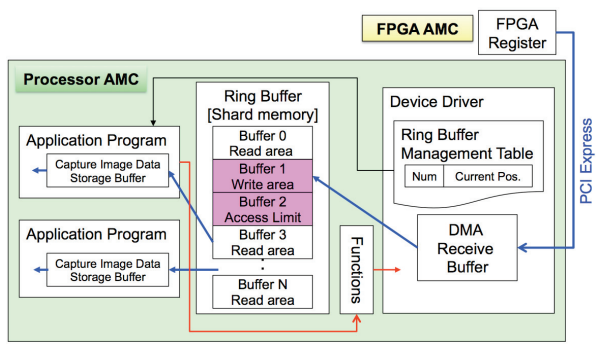

Figure 4: Data flow of captured image.

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memory. The received image data are written to the ring buffer and accessed in parallel by the user applications. Figure 4 shows the data flow of a captured image.

For the development of user applications, we provided the Linux library with features such as camera control, board settings, and operation.

Standalone Performance

We tested the performance of the system. As a result, in continuous trigger mode, we successfully captured images at up to 100 Hz, which is the maximum image rate for the 12-bit grayscale VGA-resolution camera (IMPERX Inc., IPX-VGA-120), and up to 60 Hz in external trigger mode. This meets the performance requirements for beam diagnostics at the SPring-8, which operates at 1 Hz. Furthermore, it can be used for the diagnostics of electron-beam and X-ray imaging experiments in SACLA, which operates at 60 Hz.

APPLICATION FOR THE SR INTERFEROMETER

The MicroTCA system was first applied to upgrade the image processing system for the two-dimensional synchrotron radiation (SR) interferometer that is used for the non-destructive diagnostics of the stored electron beam in the SPring-8 storage ring. The interferometer enables the simultaneous measurement of transverse beam sizes along the major and minor axes and the beam-tilt angle. The visible light emitted from the point source in the bending magnet is steered towards the interferometer by two plane mirrors, and the CCD camera subsequently captures the interference pattern. The schematic view of the two-dimensional interferometer and interference pattern are shown in Figure 5.

Currently, the interferogram from a CCD camera with analog output has been captured and processed by a conventional PC-based system that was installed 10 years ago. The horizontal and vertical visibility can be obtained by the 1D fitting calculation of the projected interferogram image. Subsequently, they are converted to beam sizes and written to a database with a 1 Hz cycle. The beam-tilt angle is derived offline from a 2D fitting calculation for an assumed elliptical Gaussian distribution. For real-time viewing of the interferogram on a large display in the central control room (CCR), we branch the analog output from the CCD camera and send the image using a video encoder module with a network interface. Figure 6 shows the current image processing system for the interferometry.

Requirements

On upgrading the image processing system, we have realized following requirements while keeping the current capabilities.

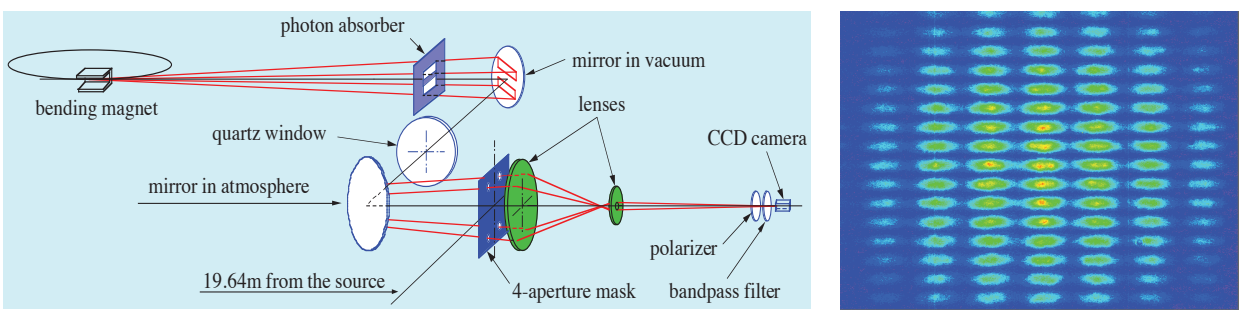
- Online measurement of the sizes and tilt angle of transverse electron beam profiles is performed by fast fitting, which uses the two-dimensional model function. The results are written to the database in a 1 Hz cycle.
- The live view function in the CCR is combined with the image processing system at more than 1 Hz.
- The control system is integrated into the Message and Database Oriented Control Architecture (MADOCA) framework [6] for the SPring-8 standard operation.

In order to meet these requirements, we have built an image processing system by applying a MicroTCA.

System Configuration

The schematic diagram of the new image processing system based on the MicroTCA is shown in Figure 7. The primary processor AMC is in charge of camera control, image transfer to both the CCR and secondary processor AMC, and 1D fitting calculation. The secondary processor AMC is dedicated to real-time 2D fitting calculation.

We have developed the control software for the image processing system using the MADOCA II framework [7], which has been developed as a next-generation control framework. In the MADOCA II framework, the messaging functionality has been extended to handle variable-length data such as image data and to perform concurrent processing of multiple messages. Using this function of MADOCA II and the ring buffer implemented in the Linux library, we have realized parallel processing for handling simultaneous image data from multiple applications. A new control GUI in the CCR was developed for camera control and image data acquisition.



a) Two-dimensional interferometer b) Interferogram

Figure 5: Schematic view of the two-dimensional interferometer and an example of observed two-dimensional interferogram at the SPring-8 storage ring.

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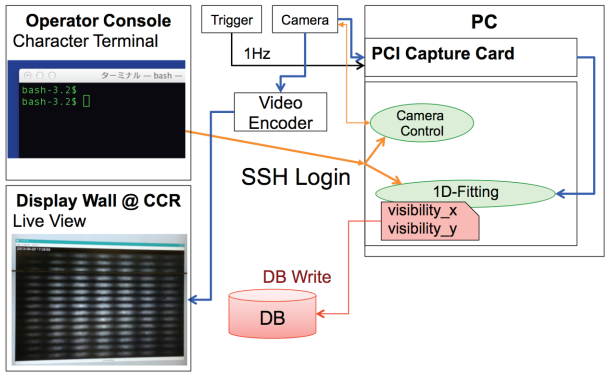

Figure 6: Schematic diagram of the current image processing system for the two-dimensional synchrotron radiation interferometer.

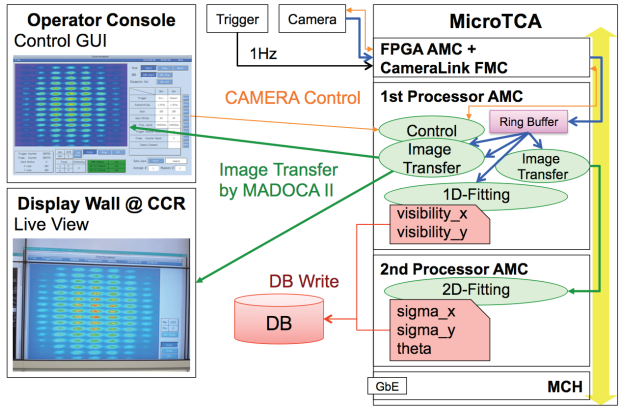

Figure 7: Schematic diagram of the new image processing system for the two-dimensional synchrotron radiation interferometer.

The live-view GUI for the interferogram image is running on large display in the CCR. It captures the image data via Ethernet with a refresh rate of 1 Hz.

In the 1D fitting calculation of the primary processor AMC, the measured horizontal and vertical visibilities are written to database in a 1 Hz cycle. The secondary processor AMC captures the image data from the primary processor AMC through backplane Ethernet, and then it measures the beam sizes and the beam-tilt angle by a 2D fitting calculation. The results are written to a database in a 1 Hz cycle.

Performance of the New System

We tested the performance of this application. Using the MADOCA II framework, the live-view display in the operator console worked at up to a 10 Hz trigger rate. The measurement of beam sizes and beam-tilt angle by a two-dimensional fitting calculation takes about 0.5 s. For parallel processing to divide the tasks between two processor modules, this system was able to perform measurements and write to the database in less than 1.0 s. Our aim is to implement this system during the SPring-8 storage ring operation.

CONCLUSION AND FUTURE PLANS

We have developed an image processing system based on the MicroTCA platform. The Camera Link FPGA IP core is newly developed using COTS products including a Camera Link FMC and a user-configurable FPGA AMC. A Linux device driver and library were also developed. The system was completed as a highly reliable, flexible, and compact solution, which resolves the disadvantages of PCs. It can be used with a wide variety of Camera Link base configuration cameras. It succeeded in capturing images at up to 100 Hz in continuous trigger mode and up to 60 Hz in external trigger mode with a 12-bit grayscale VGA-resolution camera.

This MicroTCA system has been applied to upgrade of the image processing system for the two-dimensional SR interferometer. We have developed the control software using the MADOCA II framework. We realized real-time measurement of the beam sizes and the beam-tilt angle by fast 2D fitting calculation using multiple processor modules. The results are written to the database in a 1 Hz cycle.

As future plans, we are considering the following improvements.

- Modify the manufacturer-provided IP cores, such as the DMA controller and PCI Express bridge, to support AXI4 instead of PLB connection.
- Modify the manufacturer-provided device driver to realize the support for a 64-bit OS and the use of hot-swapping.
- Realize the communication between processor AMCs via PCI Express instead of Ethernet.

We expected a further extension of flexibility and scalability by these improvements.

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