# ADVANCED LIGHT SOURCE CONTROL SYSTEM UPGRADE – INTELLIGENT LOCAL CONTROLLER REPLACEMENT*

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*Abstract*

As part of the control system upgrade at the Advanced Light Source (ALS) the existing intelligent local controller (ILC) modules have been replaced. These remote input/output modules provide real-time updates of control setpoints and monitored values. This paper describes the 'ILC Replacement Modules' which have been developed to take on the duties of the existing modules. The new modules use a 100BaseT network connection to communicate with the ALS Experimental Physics and Industrial Control System (EPICS) and are based on a commercial FPGA evaluation board running a microcontroller-like application. In addition to providing remote analog and digital input/output points the replacement modules also provide some rudimentary logic operations, analog slew rate limiting and accurate time stamping of acquired data. Results of extensive performance testing and experience gained now that the modules have been in service for several months are presented.

## INTRODUCTION

For over twenty years the Advanced Light Source at Lawrence Berkeley National Laboratory has relied on locally-developed Intelligent Local Controller (ILC) modules[1] to monitor and control low-speed analog and digital signals. The ILCs communicate with the rest of the control system through a multi-drop 2 Mb/s serial link connected to a Multibus I processor which now connects to the newer EPICS-based control system equipment. The serial links and Multibus I processor now represent a considerable bottleneck to performance and are increasingly difficult to maintain. Design effort to replace the ILCs began in 2010. The possibility of replacing the ILCs with commercial Programmable Logic Controllers (PLCs) was investigated but ultimately rejected because of the major effort in recabling to accommodate the PLC physical architecture. The decision was made to simply replace the ILCs with more modern equipment while retaining the card edge connector and signals of the original. The recabling effort was thus reduced to replacing the multi-drop serial links with 100BaseT ethernet links between the IRMs and the network switches.

## SYSTEM DESCRIPTION

The form factor of the IRM matches that of the ILC modules that it replaces. It is a 3U high and 220 mm deep Eurocard format with a 96-pin rear panel connector. The entire circuit board is mounted inside a shielding canister to reduce coupling of ambient electrical noise to the analog input and output signals. Power consumption has been reduced from the approximately 5 W of the ILC to less than 3 W. A block diagram of the IRM hardware is shown in Figure 1. The core component of the IRM is the LX9 MicroBoard based on a Xilinx® Spartan®-6 LX9 FPGA[2]. In addition to the FPGA the MicroBoard provides dynamic RAM, flash memory, a 100BaseT ethernet interface and input/output lines used to communicate with the other IRM components. The FPGA firmware provides a Microblaze[3] embedded processor with additional peripheral firmware modules to support communication with the components on the carrier board on which the FPGA microboard is mounted.

The ranges of the analog channels and the signal levels of the digital channels on the backplane connector match those of the ILC. The analog to digital converter (ADC) used in the IRM is an Analog Devices AD7606 6-channel, 16-bit device. A notable feature of this chip is its ability to sample and average 64 values for each 'convert' request. The equivalent sampling frequency for the IRM is thus increased from 1 kHz to 64 kHz. This reduces the effects of high frequency noise and greatly reduces aliasing of high frequency components. Four of the channels are driven by signals from the backplane connector conditioned by a differential amplifier providing up to 200 V of common mode signal. Another channel is used the measure the analog signal from a sensor measuring the ambient temperature. The digital to analog converter (DAC) is an Analog Devices AD5764 4-channel, 16-bit device. The port expander chips are Maxim 7301 28-bit devices. The port expander connected to the backplane operates from a +5 V supply. The digital channels are arranged as six banks of 4 bits each. Four of these banks are configurable as inputs or outputs. The other two banks are always inputs from the backplane.

The FPGA board is mounted on the main IRM circuit board so that the RJ45 ethernet connector and the micro-USB console connector are accessible through the front panel. A full color 64 row by 96 column OLED front panel display is used to show the status of the digital input output signals, the DAC and ADC voltages, the value read from the temperature sensor and the status of the network connection to the EPICS Input/Output Controller (IOC) application to which the IRM is connected. Front panel controls consist of a pair of rotary 16-position switches used to set the IP address of the IRM and a single push button. To prolong its life the OLED is shut down after more than 30 minutes of inactivity. Pressing the button turns the display

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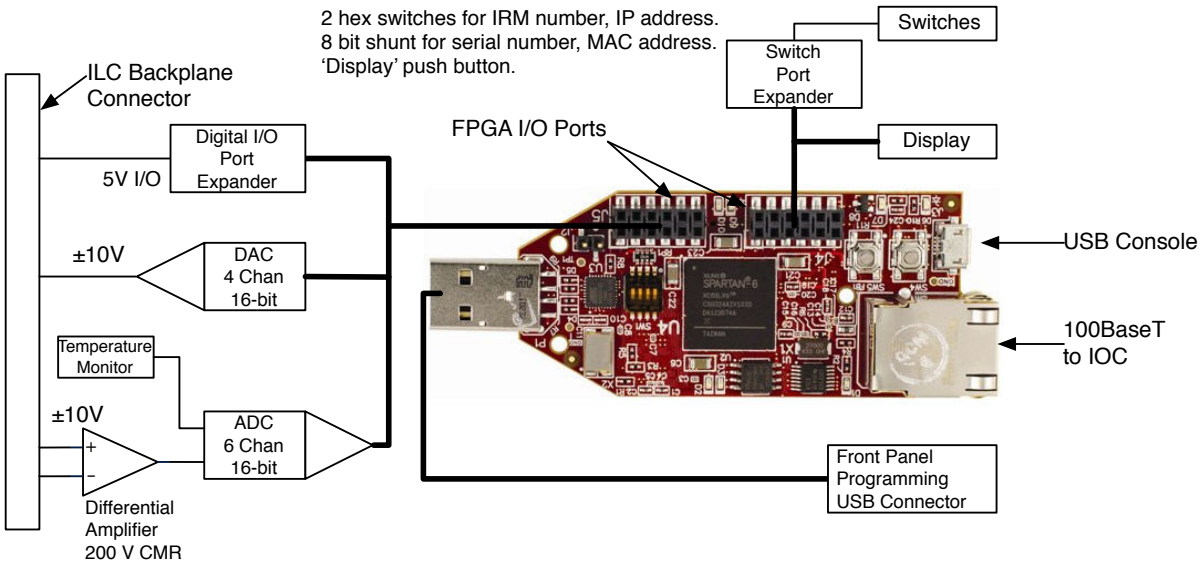


Figure 1: IRM hardware showing commercial FPGA board and added components.

on for another 30 minutes. Pressing and holding the button for more than 5 seconds puts the IRM into programming mode in which updated FPGA firmware or software can be loaded into the microboard flash memory using a TFTP server in the FPGA. Holding the button down during power-up causes the IRM to enter calibration mode when attached to a special calibration fixture. All ADC and DAC gains and offsets can be set using this fixture and a single precision voltmeter.

An ILC module can act as an IEEE-488 general purpose bus controller. This capability has been dropped from the IRM since the few devices at the ALS which are still controlled using this mechanism can be connected to the control system through ethernet-based IEEE-488 controllers.

The IRM software for the Microblaze processor was produced using the Xilinx Software Development Kit and the Standalone board support package. No operating system layer is present. The execution environment is single-threaded and driven by interrupts from a 1 kHz timer to set the sampling rate and from the ethernet controller to communicate with the EPICS IOC. The networking calls use the raw Lightweight Internet Protocol (LWIP) interface. This provides good performance with very little overhead.

## NETWORK PROTOCOL

The IRM receives all packets on UDP port 7094. All IRM packet transmission is from this port to whatever ports have been chosen by the IOC. Multibyte values are sent in the order of the IOC architecture so no byte swapping is needed at the IOC. Byte swapping, if necessary, is performed for all packets at the IRM. All packet components are 16-bit. This makes the IRM byte-swapping routine very simple. 32-bit values are sent as two separate 16 bit words explicitly labelled Hi and Lo.

A simple receive-only network time protocol (NTP) client is implemented in the IRM firmware. The lab time server machine broadcasts an NTP time synchronization packet 64 seconds. The latency in the delivery of these broadcast packets is low enough to allow the IRMs to maintain time values within 1 ms of other NTP clients at the facility and to within 100 $\mu$s of each other.

- Endian-detect number.
- 32-bit value of integer number of seconds since EPICS epoch.
- 16-bit value of fraction of a second, in 20 s steps, since above integer number of seconds.

Commands and replies share the same packet structure. There are special packets for device identification replies and for timer histogram readout replies. After sending a command the IOC waits one second for a reply. If no reply is received within this time the command is retransmitted. Five attempts are made after which the IOC reports a communication error.

- Endian-detect number.
- 16-bit command/reply code (e.g. `SET_BOOLEAN`, `CLEAR_BOOLEAN`, `SET_DAC`).
- 16-bit command/reply sequence number.
- 16-bit channel number.
- 32-bit value.

On startup the IOC sends a subscribe packet to the IRM containing:

- Endian-detect number.



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- A 16-bit value of which 4 bits are used to specify the direction of the bidirectional digital I/O bits.
- Four 32-bit values setting the maximum slew rate of the analog outputs.
- Four groups of two 32-bit values (output bitmap and enable bitmap) and one 16-bit value (timer) configuring the software seals which are simple IRM state machines used to inhibit setting or clearing of digital outputs until some particular set of digital inputs conditions is met.

Upon receipt of a subscribe packet the IRM begins sending data packets to the IOC at a rate of 50 packets per second:

- 16-bit packet sequence number.
- 16-bit IRM identification number as set by the IRM front-panel rotary switches.
- One 32-bit value and one 16-bit value containing the time value from the most recent time synchronization broadcast.
- 32-bit sample index counter value when the last sample of this packet was acquired.
- 16-bit IRM temperature.
- 16-bit IRM status (Calibrated, Power OK).
- 32-bit bitmap of digital I/O values that have changed state since the final sample of the previous data packet.
- 32-bit bitmap of digital outputs before software seals have been applied.
- 32-bit bitmap of digital outputs after software seals have been applied.
- 16-bit value of which 4 bits are used to indicate the direction of the bidirectional digital I/O bits.
- The value of the 32-bit 100 MHz tick counter when the last sample in the packet was acquired. The tick counter is reset when a rising edge is detected on the INT1 input. This allows a timing system event receiver to provide fine time synchronization of IRM data.
- 20 data samples, each containing four 16-bit ADC values, four 16-bit DAC values, and a 32-bit bitmap of digital port state.

## HARDWARE UPDATES

A prototype IRM built using evaluation boards available from the manufacturers of the ADC and DAC chips was constructed. The prototype proved that the chosen components were capable of meeting or exceeding the performance of the ILCs. Initial development of the FPGA firmware was somewhat troubling in that the implementation of the on-chip processor and associated peripherals consumed every logic slice of the LX9 FPGA. This was unacceptable since it allowed no room for further additions to the firmware. The solution to this problem was quite simple. The Spartan 6 LX25 chip has the same pinout and footprint as the LX9 but has over twice the number of logic elements. A custom version of the microboard was purchased with an LX25 chip in place of the LX9.

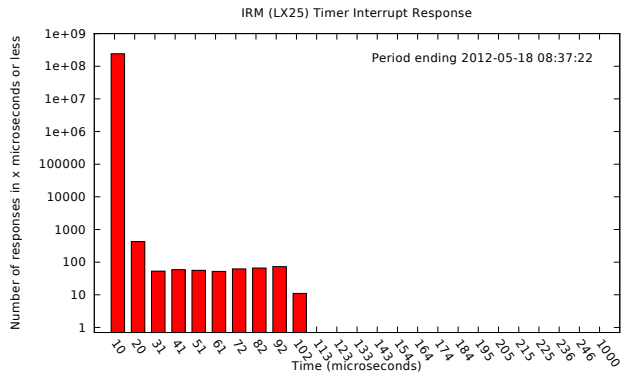


Figure 2: Timer interrupt latency for LX25 hardware.

The increase in available logic elements allowed the implementation of the on-chip Microblaze processor to be improved in several ways.

- The instruction and data cache memories were doubled in size, from 8 kB to 16 kB each.
- The data cache architecture was changed from write-through to write-back. This allows main memory write operations to be deferred until the memory is otherwise idle.
- Instruction stream readahead was implemented. This increases the chances that an instruction will be in the cache when needed.
- Cache buffering was increased so that the eight most recently flushed cache lines were held.

Figure 2 shows the latency for the LX25 hardware with the firmware improvements noted above. The worst case response time is less than 102 $\mu$s. This represents a considerable improvement over the LX9 hardware which exhibited a worst case response time of 164 $\mu$s. The result is that jitter in the sampling of the analog and digital inputs has also dropped by this amount.

An additional benefit of the additional resources provided by the LX25 was that the extra logic elements allowed an NTP time synchronization block to be added to the firmware.

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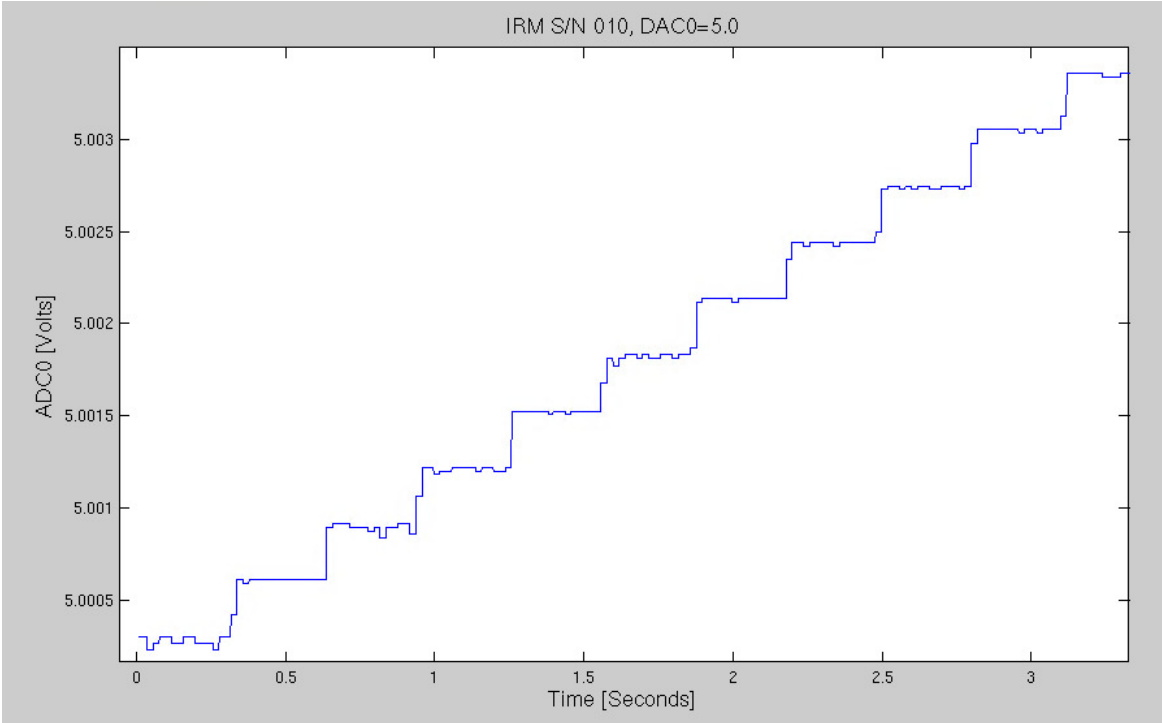


Figure 3: Analog I/O performance.

## ANALOG INPUT/OUTPUT PERFORMANCE

To provide an end to end test of the performance of the analog input/output hardware an analog output channel was externally looped back to an analog output channel and the value read from was recorded as the output was swept through a range of values using the ramp output feature. The output ramp rate was set to 1 mV/ms and the values of 20 consecutive analog input samples were averaged resulting in a sample rate of 50 Hz. A plot of the portion of the acquired data is shown in figure 3. Several points are apparent. The first is that the individual DAC steps are clearly visible. This is a result of the increase in effective number of ADC bits provided by the sample averaging. The next point that can be inferred is that there is very little noise present in the ADC readings at each DAC step. It is clear that the DAC outputs are quiet and that the ADC reading noise is well within one ADC count.

An independent test of the noise and drift present on the DAC outputs was performed by using a precision voltmeter to measure the DAC signal over an 18 hour period. In this time the noise was found to be less than 5 $\mu$V RMS and the drift less than 15 $\mu$V. Both these values are far below a single DAC step of approximately 305 $\mu$V.

## CONCLUSION

Results of tests using the prototype show the performance of the analog input and output channels to be superior to those of the ILCs. The front panel display allows for quick monitoring the status of the module and the level of all I/O signals. The new system provides full logging of every sample for up to 10 days as well as providing EPICS process variables for every analog and digital input and output point. At the time of writing 110 modules have been in production use for over eight months. In that time no hardware issues have occurred. Over $75 \times 10^9$ data logging packets have been received with no packet loss during machine setup and user operations. In addition, 99.9998% of commands sent to the modules were acknowledged immediately and the remainder were acknowldedged after the first retry.

## REFERENCES

[1] S. Magyary, M. Chin, C. Cork, M. Fahmie, H. Lancaster, P. Molinari, A. Ritchie, A. Robb, C.Timossi, *Advanced Light Source Control System*, Proc. of the 1989 IEEE Particle Accelerator Conference, Chicago, IL, March, 1989, pp. 74–76.

[2] *Xilinx Spartan-6 FPGA LX9 MicroBoard User's Manual*, Avnet Incorporated, 2211 South 47th Street, Phoenix, AZ, 85034.

[3] *MicroBlaze Processor Reference Guide*, Xilinx Incorporated, 2100 Logic Drive San Jose, CA, 95124.



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