DEVELOPMENT OF A FRONT-END DATA ACQUISITION SYSTEM WITH A CAMERA LINK FMC FOR HIGH-BANDWIDTH X-RAY IMAGING DETECTORS

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Abstract

We have developed a new front-end data acquisition system (DAQ) for synchrotron radiation experiments at the Super photon ring 8 GeV (SPring-8) in Japan. X-ray imaging detectors are indispensable for synchrotron radiation experiments, and their performance is being continuously enhanced. Further, recent experiments tend to use various types of detectors. Therefore, the proposed front-end DAQ system should satisfy to need for a relatively high data rate and support various interfaces of the X-ray imaging detectors. This system is based on FPGA with a high-bandwidth transceiver and an FPGA mezzanine card (FMC). The novel detector that is under development at SPring-8 is selected for one of applications. Since the first phase of the detector adopted a camera link (CL) interface, we developed a front-end DAQ system with a CL FMC and achieved stable operation with 4.5 Gbps high-bandwidth. In this paper, we will describe the design and evaluation results of the proposed front-end DAQ system with a CL interface. Moreover scalable upgrade schemes of DAQ system to follow further detector upgrades will be reported.

INTRODUCTION

X-ray two-dimensional imaging detectors are indispensable for synchrotron radiation experiments, such as coherent X-ray imaging, spectroscopy, and time-resolved experiments. In order to obtain more detailed information of the samples, detectors are continually upgraded to achieve a larger number of pixels, a wider dynamic range, and a higher frame rate.

The Super photon ring 8 GeV (SPring-8) site has two types of accelerators for synchrotron radiation experiments. One is SPring-8 that is an accelerator complex with an 8-GeV electron storage ring and around 60 synchrotron radiation beam lines along a ring having a circumference of 1.5 km. The other is the SPring-8 angstrom compact-free electron laser (SACLA) that is an X-ray free-electron laser (XFEL) facility that can produce high peak brilliances and femtosecond-order X-ray pulses [1]. X-ray imaging detectors are also essential in both synchrotron radiation and XFEL experiments. Since the SPring-8 site has a large number of beam lines, various type of detectors, the commercial and the ones developed in-house, have been used.

As a next-generation detector, the silicon-on-insulator photon imaging array sensor (SOPHIAS) is under development [2]. The use of the silicon-on-insulator (SOI) production method leads to a larger number of pixels and a higher frame rate. Moreover, this detector is based on the multi-via concept in which each implant region is connected to the readout circuit by a metal via. A biased charge collection by adjusting the number of via connections helps to achieve a wider dynamic range. The detector of the first phase will be provided for synchrotron radiation experiments in 2014. After the first phase, phase-by-phase upgrades are planned as further high-bandwidth of data transmission from 4 Gbps to 20 Gbps and increment of sensor components of a detector from 2 to 40 sensors (table 1).

Thus, detector upgrades drastically increase the output bandwidth. However, the upgrade of the DAQ system as well as detector upgrades is also important to improve the overall results of the synchrotron radiation experiments. Therefore, we have developed a new front-end DAQ system.

REQUIREMENTS FOR NEW FRONT-END DAQ SYSTEM

Sensor Improvement of X-ray Imaging Detector for SACLA Experiments

Table 1 shows the specifications of a single sensor of SOPHIAS detector and front-end DAQ. Since the specifications of SOPHIAS in the final phase are under consideration, the sensor specifications are given as possible values and the front-end DAQ specifications remain to be decided (TBD). SOPHIAS' first phase adopted the camera link [3] protocol, which is also used as a machine vision standard. Camera link has five configurations, namely lite, base, medium, full, and 80-bit, corresponding to the data transmission bandwidth. The full configuration is adopted for SOPHIAS. The required bandwidths of front-end DAQ are considered an actual experimental environment such as a beam shot repetition of an accelerator and a data format of a sensor electronics output. For the first phase of SOPHIAS, the required bandwidth considers an accelerator repetition of 30 Hz and the data bandwidth of factor four because four types of images are acquired for single beam shot, these are "two types of signal gain configuration" and "signal and background data acquisition." For the final phase of SOPHIAS, a wider dynamic range and a higher frame rate, will be applied. Moreover, its throughput will exceed the

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ISBN 978-3-95450-139-7

maximum bandwidth of the camera link protocol, 6.4 Gbps at the 80-bit configuration. Therefore, we should change the sensor interface in the future.

Table 1: Sensor and Front-End DAQ Specifications

	SOPHIAS (1st)	SOPHIAS (Final)
Sensor		
No. of pixels	~2M	~2M
Depth (bit)	16	16~32
Frame rate	60 Hz	<300 Hz
Experimental conditions		
Frame rate	30 Hz	TBD
Data size for one frame	~16 MB (4 types of data for one shot)	TBD
Detector composition	2 sensors	~40 sensors
FE DAQ		
Required bandwidth /sensor	3.7 Gbps	~20 Gbps
Sensor interface	CL full configuration	TBD
Bandwidth	<5.44 Gbps	TBD
Computer interface	PCI express gen2 × 8	TBD

Requirements and Conceptual Design

The requirements for a new front-end DAQ system are "high-bandwidth data transmission" and "support for various types of input/output interfaces."

- High-bandwidth of data transmission
  The abovementioned system requires a current bandwidth of less than 10 Gbps. However, a maximum of 20 Gbps will be needed in the future. Both the input and the output throughputs should be considered for the entire front-end DAQ system.

- Flexible and scalable composition
  As the SOPHIAS upgrade plan indicates, the input and output interfaces can be changed to achieve the final specification. If the throughput of the sensor will exceed the Camera Link specification, a new interface which supports required bandwidth, should be adopted. Further, if the detector composition will be scaled up to 40 sensors, the board platform should be changed from a direct connection with PC platform to a backplane based bus type connection. Since a drastic change in the FE-DAQ system should be avoided, we need to consider a good scheme to exchange interfaces easily.

Figure 1 shows the conceptual design of the proposed DAQ system for a basic single data stream. If a detector is composed of many sensors, we can follow it by increasing the number of data streams. Since a front-end DAQ system is located between a sensor and the computing platform, the input and output interfaces are the connections with the sensor and the computing platform, respectively. The proposed front-end DAQ system is based on an exclusive data acquisition board with a programmable logic device, memories, and interfaces. The key function is a separation of a FPGA carrier board and input/output interfaces. If the sensor output interface or a computing platform connection will be changed, the DAQ system can follow only to develop an appropriate interface card.

Figure 1: Conceptual design of proposed DAQ system.

Hardware selection

We considered not only a limited application but also a general one for supporting various detectors and the replacement of interfaces. In order to reduce the development costs and time, we adopted a commercial off-the-shelf (COTS) method. By combining some COTS products, we can develop various applications without any board production.

An FPGA with a multi-gigabit transceiver (MGT) is adopted for high-bandwidth data handling. Since support for a variety of input/output interfaces is required, an FPGA mezzanine card (FMC) [4], which is standardized as the VITA 57, is adopted for connection between the FPGA and the input/output interface. The bandwidth performance of FMC is 10 Gbps per signal and 40 Gbps with a carrier card and satisfies the bandwidth requirement of around 20 Gbps for SOPHIAS' final phase.

Table 2 presents the specifications of the selected FPGA board. The board has a PCI express form with an FPGA and two FMCs. The FPGA has 24 transceivers with a maximum bandwidth of 6.5 Gbps. The FMC is of the HPC (high-pin-count) type with 400 I/Os including eight transceivers.

Feasibility Study

First, we confirmed that the selected board satisfied the required performance, i.e., had a "high bandwidth of 20 Gbps" and provided "support to various types of input/output interfaces." Therefore, we developed an evaluation system and evaluated its performance. For

ISBN 978-3-95450-139-7

checking whether various types of input/output interfaces were supported, we selected three types of FMCs and used transmission protocols. The specifications of the selected FMCs and the measured performances are presented in Table 3. As a result, we found that the selected board FMCs satisfied the required bandwidth using only one pair of FPGA boards by switching the FMCs [5].

Table 2: FPGA Board Specifications

Device	Specification
Platform	PCI express
FPGA	XC6V-LX240T-2FFG1759
Multi-gigabit transceiver	24 lanes × 6.5 Gbps
PCI express	× 8 lanes (Gen 2)
FMC connector	HPC (high pin count) × 2
Memory	DDR3 SDRAM ×2 2-GB SO-DIMM supplied

Table 3: Specifications and Measured Performances of Evaluated FMCs

FMC	Physical layer	Protocol	Measured bandwidth
FMC A	SFP+ (4ch)	AURORA	19.7 Gbps
FMC B	QSFP+ (2ch)	AURORA	19.7 Gbps
FMC C	SFP+ w/ 10-GbE PHY	XAUI	9.8 Gbps

DEVELOPMENT OF CAMERA LINK SYSTEM FOR SOPHIAS' FIRST PHASE

Since the selected devices for a new front-end DAQ system satisfied the requirements of synchrotron radiation experiments, we began to apply the evaluated devices to actual X-ray imaging detectors. Our first target is the first phase of the SOPHIAS detector. The actual data throughput is 3.7 Gbps with Camera Link full-configuration for SOPHIAS 1st phase. The connection between the front-end DAQ system and a computing platform is changed to PCI express with eight lanes of 5 Gbps.

The development is based on the FPGA board described in the previous section. The basic DAQ stream is already implemented by the feasibility study including the board for a computing platform data stream via PCI express [6]. Therefore, we need to develop only the camera link part of the physical interface and the FPGA logic.

Camera Link Interface FMC

The camera link interface FMC should follow two standards, Camera Link standard and FMC standard. For this reason, an interface FMC should implement the serializer/deserializer chips recommended by the camera link standard with a standard form of FMC board. We developed such a board in-house because there is no appropriate board in COTS lineups. Figure 2 shows the developed Camera Link FMC.

The developed camera link interface is also considered for use in other FMC carrier boards. Signal level shifters were located between the camera link chip output and FPGA I/O for adjusting the I/O signal level. Moreover, support the external signal pins for general-purpose use, which triggers the beam shot from an accelerator to synchronize data acquisition with beam shots.

For a detailed and efficient evaluation, both the sender and the receiver interfaces were developed.

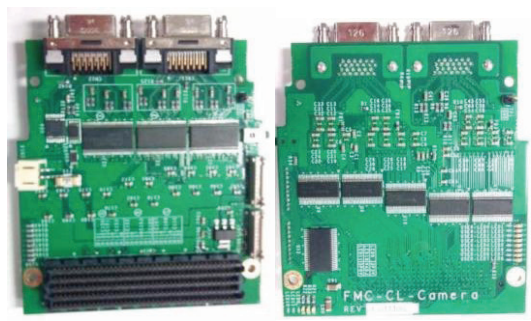

Figure 2: Developed Camera Link FMC.

Logic Implementation

Figure 3 shows the schematic representation of the logic implementation. The camera link logic was newly developed, and other parts were reused with slight revisions. Since camera link has many data acquisition configurations called the camera link modes, we implemented almost all these modes for supporting various commercial cameras.

Evaluation

We carried out two types of evaluations, that of a basic camera link function and of a connection with actual sensors/cameras.

Basic evaluation of camera link functions:

We applied Camera link functions and performance tests. Since camera link has more than twenty configuration modes, a variety of operation clocks, and a selection of valid signal modes, we developed a camera link sender FMC. For using both the developed sender and receiver FMCs, we tested more than 300 combinations of these functions by using the developed automated checking application.

ISBN 978-3-95450-139-7

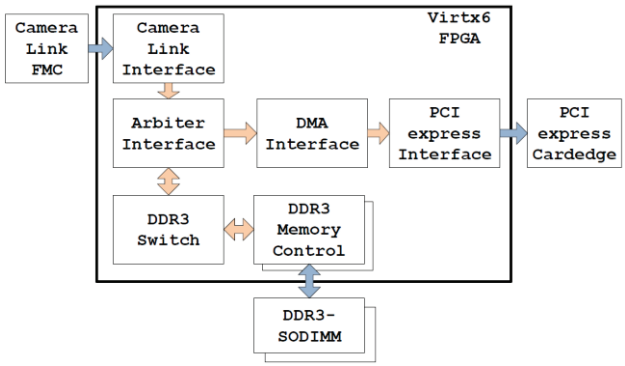

Figure 3: Schematic representation of FPGA logic implementation.

Connection with actual sensor and cameras:

Actual sensors and commercial cameras were connected with the front-end DAQ with a camera link sender FMC (Fig. 4). For a SOPHIAS sensor, we checked the camera link data transfer performance and the camera control commands using the camera link serial communication function. For the data transfer test, a data frame rate of 16MB/frame and 35 Hz corresponding to 4.5 Gbps bandwidth, which exceeds the required frame rate of 30 Hz, exhibited the required performance. Further, a long-term stability check, carried out for around 12 hours and 300 million frames, yielded good performance results. Moreover, several commercial sensors, Amidec OPAL2000 and pco.edge scientific CMOS (sCMOS), were checked. sCMOS can perform with 8-bit and 10-Tap camera link modes that have a maximum bandwidth of 6.4 Gbps.

SUMMARY

We developed a front-end DAQ system for X-ray imaging detectors used for synchrotron radiation experiments at SPring-8 and SACLA. The system is composed of FPGA and FMC. Further, we confirmed that it satisfied the requirements of a high bandwidth and supported a variety of input/output interfaces. We developed a camera-link-based front-end DAQ system for actual sensors and cameras. The developed sensor, the first phase of SOPHIAS, and several commercial cameras were evaluated and found to exhibit good performance. The development followed the COTS method, and we expect this COTS-based system to operate stably in synchrotron radiation experiments.

FUTURE PLAN

The first phase of the SOPHIAS detector is planned to start operation for user experiments in 2014. We will continue to develop additional functions except for a camera link data stream: beam trigger and shot information management. Then, the entire DAQ system will be introduced and will consist of the SOPHIAS detector, front-end DAQ, and back-end DAQ system.

For final phase of the SOPHIAS detector, we started some studies of a further high-bandwidth data transmission and a new board platform such as a backplane based one with bus connections.

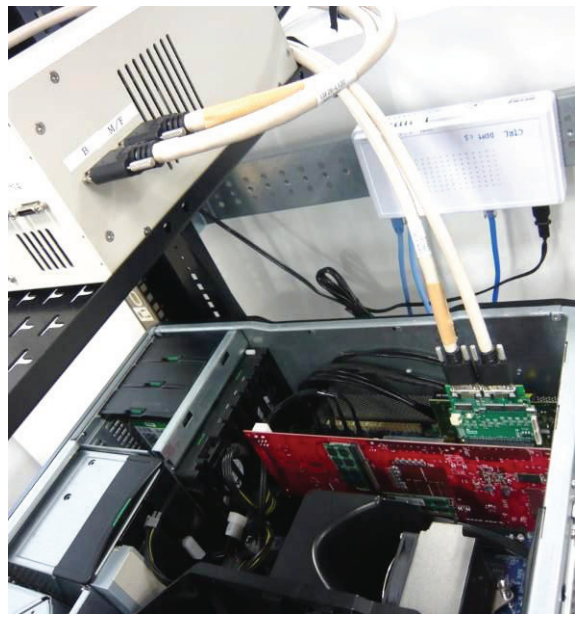

Figure 4: Test bench system for connecting with the interface device of SOPHIAS.

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ISBN 978-3-95450-139-7