DESIGN OF FAST MACHINE PROTECTION SYSTEM FOR THE C-ADS INJECTION I

Fang Liu, Jun Hu, XiaoShan Jiang, Qiang Ye, IHEP, Beijing, China
Guanghua Gong, Tsinghua University, Beijing, China

Abstract

In this paper a new fast machine protection system is proposed. This system is designed for the injection I of C-ADS which fault reaction time requires less than 20 us, and the one minute down time requires less than 7 times in a whole year. The system consist of one highly reliable control network based on a control board and some front IO sub-boards, and one nanosecond precision timing system using white rabbit protocol. The control board and front IO sub-board are redundant separately. The structure of the communication network is a combination structure of star and tree types which using the 2.5 GHz optical fiber links the all nodes. This paper pioneered the use of nanosecond timing system based on the white rabbit protocol to determine the time and sequence of each system failure. Another advantage of the design is that it uses standard FMC and an easy extension structure which made the design is easy to use in a large accelerator.

INTRODUCTION

The injection I of ADS (Accelerator Driven Sub-critical System) is being constructed in institute of high energy physics, China [1]. How to ensure the safe and stable operation of the injection, the fast protection system has played a crucial role. The protection system needs to make a quick decision on the current failure. When a general failure, the system needs to quickly adjust the system without stopping and set the working state to the normal mode. When a serious fault, it is necessary to quickly send out a signal and shutdown the whole system. The system also cans storage the statement before and after the fault. Through the storage of information the staff can quickly rule out the reason of occurrence failure [2].

FAST MACHINE PROTECTION SYSTEM FRAMEWORK

ADS fast protection system is composed of main control board, some front IO sub-boards, supervisory computer and one nanosecond precision timing system. The system framework is shown in Fig. 1.

Front IO sub-board monitors the 24V or 5V switch signal from the LLRF, PS, Vacuum, RFQ and other critical points. When the monitored points occur error, it sends the error signal to the main control board through optical fiber. The signal contains the time information that is labelled by the White Rabbit system. The main control board analyses and judgments the error through the stored fault tree. Then, it issued the processing results to the front IO sub-boards. Meanwhile, the main control board

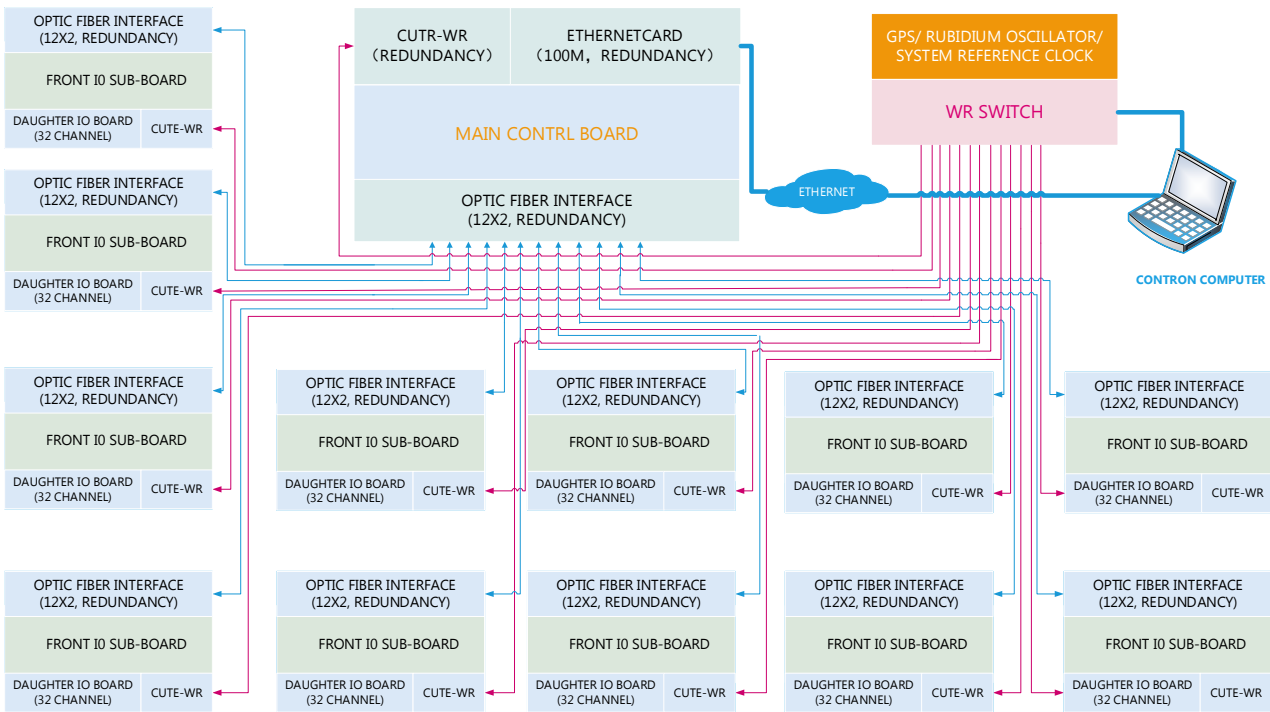

Figure 1: System Framework.

ISBN 978-3-95450-148-9

record the error, process the result and send it to the supervisory computer.

The whole fault reaction time requires less than 20us, including the monitor reaction time, transmission time and processing time.

The framework of the network is a star and tree combination structure. A main control board can control 12 block IO sub-board, and an IO sub-board can manage 32 inputs and 32 outputs separately. It will form a 384 nodes network. The framework shows in Fig. 2. When we need a greater network, we can link tow showed network (Fig.2 showed). It can reach 4068 nodes. If we want to a much bigger one, we can cascade again. So it is very suitable for Multi-node large accelerator. Another advantage of the framework is it save the signal transition time cost in each node. It just need through three nodes from one node to another node.

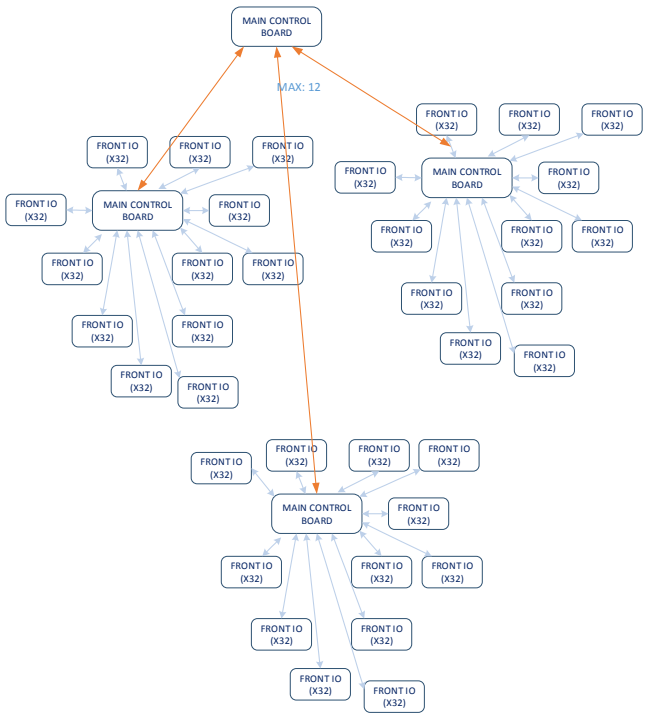

Figure 2: Network framework.

FRONT IO SUB-BOARD

The front IO sub-board use a 2.5 U box, each board can be placed independently. The input voltage is 220V alternating current. The Fig. 3 is a schematic diagram of the front IO sub-board. The front IO sub-board uses the motherboard and daughterboard design. The motherboard is responsible for power processing, logical processing, cache and data transmission. The daughter board is responsible for the acquisition and transmission of the front-end switch quantity.

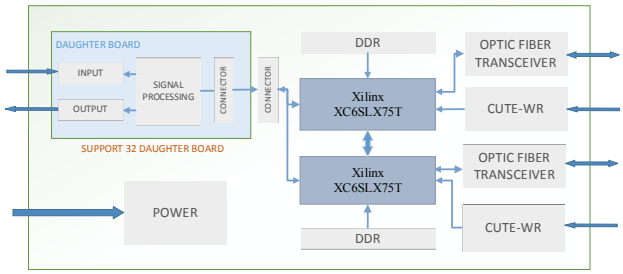

Figure 3: Schematic diagram of the front IO sub-board.

Mother Board

The mother board uses XC6SLX75T-3FGG676I FPGA as the main processor, and communicates with 32 daughterboard through 32 cables. We use the embedded Rocket IO module in FPGA to implement the optic fiber transceiver [3]. The transmission protocol is Aurora 8B/10B. The line rate is 2.5 Gbps. FPGA logic is responsible for the packing and unpacking of parallel data. At the same time, the FMC interface is used to connect the White Rabbit's timing system. And the DDR2 1 GB is used to cache the data.

In order to improve the reliability, the motherboard uses the method of watchdog, redundancy FPGA, DDR and optic fiber transceivers. The reliability of transmission between motherboard and daughterboard is guaranteed by the link showed in Fig. 4. Normal work, the master FPGA on motherboard receive data from 4 and send data to daughterboard from 3, the slave FPGA will also receive the same data from the daughterboard through 7 as a copy one and receive the feedback data from daughterboard through 8 as the verification of the master FPGA send data success. At the same time，the master and slave FPGA will check the work status for each other, and timely send control state to the back-end processing module.

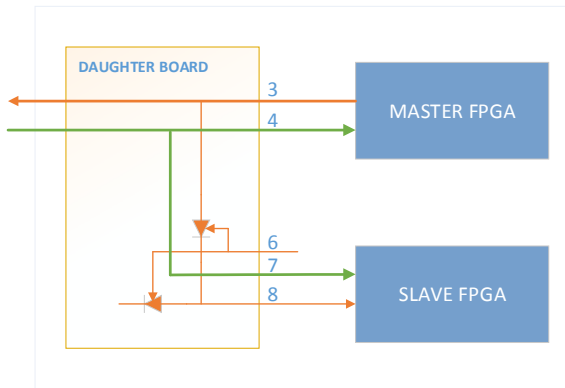

Figure 4: The link between motherboard and daughterboard.

Daughter Board

In order to ensure the link between the fast protection system and monitored system, we design three type boards: 24V optocoupler isolation board, 5V optocoupler isolation board and optical transmission board. The line

ISBN 978-3-95450-148-9

rate of each board requires not less than 3Mbps. The board logic is defined as follows:

- ***24V optocoupler isolation board:*** level greater than 12V as normal, as the error level is less than 5V.
- ***5V optocoupler isolation board:*** level greater than 3.5V as normal, as the error level is less than 0.8V.
- ***Optical transmission board:*** according to the optical fiber signal definition "1" as normal, "0" as an error.

The 24V optocoupler isolation board uses TND316S chip as a driver, the 5V optocoupler isolation board uses SN54AC245. The optocoupler chip is FOD8001. The fiber optical transmitter uses HFBR-1414TZ and HFBR-2412TZ. When the signal is transmitted over a long distance or high voltage, the signal will be transmitted through the optical fiber.

MAIN CONTROL BOARD

The main board also use a 2.5U box. The function is receiving data from front IO sub-board, judging and processing the data, sending control command and storing system useful information. The Fig. 5 is a schematic diagram of the main control board.

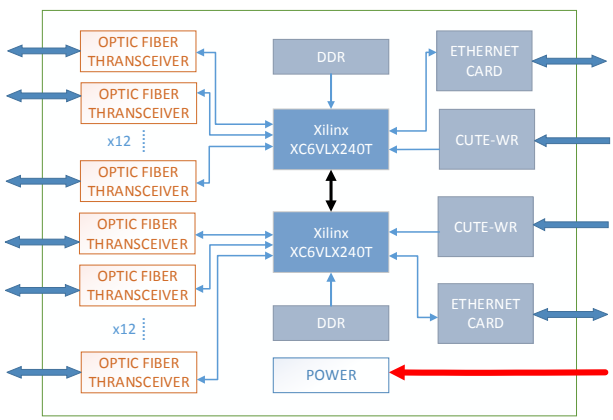

Figure 5: Schematic diagram of the main control board.

The main control board uses Xilinx XC6VLX240T FPGA. The board can receives12 channel signals from the front IO sub-board. It will complete the monitor, analysis, packing and feedback in the FPGA. The status log information will regularly sent to upper computer by a 100Mbps Ethernet sub-card using a FMC interface.

The types of optic fiber transceiver, the transmission protocol, DDR, White Rabbit module are all as same as the front IO sub-board.

In order to improve the reliability, the main control board also uses redundancy design including FPGA, optic fiber transceiver, Ethernet and White Rabbit. The double FPGA will timely check the status of each other. The status includes voltage and temperature information, the current FPGA state and the logic confirm. When we detect the master FPGA in an abnormal mode, the slave FPGA will automatically take over the function of the master FPGA and report the error.

WHITE RABBIT SYSTEM

The White Rabbit timing system is a less than 1ns accuracy, 10ps precision and suitable for long-distance transmission timing system. It can receive GPS, rubidium oscillator and reference clock signal [4].The framework of ADS injection I White Rabbit timing system is shown in Fig. 6.

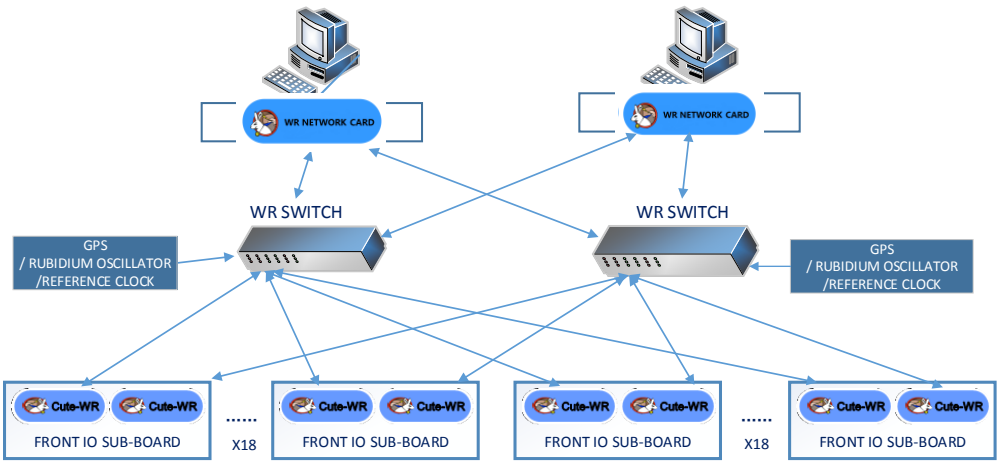

Figure 6: Framework of White Rabbit timing system.

The network is mainly composed of a white rabbit switch, some front end Cute-WR modules and a white rabbit protocol network card that responsible for the linking to computer. According to the final construction requirement, the switch can choice GPS, rubidium oscillator or the accelerator timing reference clock. The Cute-WR module is the terminal module of the system. It can receive clock and time signal from the switch. A switch can link 18 Cute-WR modules. For this system, we use 13 Cute-WR modules, 12 of which are used in the link of 12 front IO sub-boards, and the other for main control board. The entire WR network uses backup design. It guaranteed the system reliability.

ISBN 978-3-95450-148-9

CONCLUSION

According to the reliability and safety requirements, this paper presents a new scheme of accelerator machine protection system. It can make the protection action time less than 20 us and it use sub-nanosecond timing system as the clock and time module, which make it possible to determine the errors occur time and the error sequence. And each node of the system is an independent and easy organized one. It made the system with good integration and scalability.

REFERENCES

[1] Jingyu Tang and Zhihui Li (ed.), Conceptual physics design of the C-ADS accelerators, IHEP-CADS Report/2012-01E.

[2] C.Sibley, "Machine Protection Strategies for high power accelerators", IPAC2003, Portland, USA, p.607 (2003).

[3] Xu Wenbo and Tian Yun， Xilinx FPGA：Development and Application (second edition).

[4] Open hardware repository, http://www.ohwr.org/projects/white-rabbit

ISBN 978-3-95450-148-9