CUSTOM HARDWARE PLATFORM BASED ON INTEL EDISON MODULE*

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Abstract

The Computer-on-Module (COM) approach makes cutting edge technology easily accessible and lowers the entry barriers to anyone prototyping and developing embedded systems. Furthermore, it is possible to add all the system specific functionalities to the generic PC functions which are readily available in an off-the-shelf core module, reducing the time to market and enhancing the creativity of system engineers. The purpose of this paper is to show a custom hardware platform based on the tiny and low power Intel Edison compute module [1], which uses a 22 nm Intel processing core and contains connectivity elements to ensure device-to-device and device-to-cloud connectivity. The Intel Edison carrier board designed is expected to act as a local intelligent node, a readily available custom EPICS IOC [2] for extending the control reach to small appliances in the context of the SPES [1] project. The board acts as an Ethernet to RS232/RS422 interface translator with Power-Over-Ethernet supply and network booting as key features of this platform. The x86 architecture of the Edison makes standard Linux software deployment straightforward. Currently the board is in advanced prototyping stage.

INTRODUCTION

Nowadays embedded systems are commonly found in consumer, industrial, automotive, medical, commercial and military applications. An embedded system is hardware and software designed to perform specific tasks but we introduce here a custom hardware platform that is based on a commodity computing platform, thus partially bridging the gap between custom development and commercial off-the-shelf personal computers. The possibility to build an embedded system around a Computer on Module, for example a commercial and highly compact computing platform, represents a step towards a general purpose embedded system.

BOARD OVERVIEW

Particle accelerators need a distributed control network capable to reach devices of different types and requirements. In this context a certain effort is required for embedding the control of a single appliance or a small group of appliances. The custom hardware platform object of this paper has been inspired by the necessity to extend the control reach to small groups of magnet power supplies around the SPES accelerator, actually in construction at LNL (Laboratori Nazionali Legnaro) [3]. Magnet power supply boxes are accessible via serial buses, so we need a low power and low cost microprocessor board running the EPICS IOC software together with one or more RS232/RS422 interfaces. Although the magnet control is the target application, we realized that a more general approach opens the possibility of embedding different instrumentation around the accelerator, preserving the investment.

A Desktop PC

This embedded system is built around the Intel Edison compute module which integrates a 22 nm Intel Atom Processor dual-core 500 MHz. Lot of general purpose PC functionalities like a Wi-Fi dual-band (IEEE 802.11a/b/g/n) controller, an USB 2.0 OTG (On The Go) controller and 40 GPIO (General Purpose Input Output) configurable as I2C, I2S, SPI, SD card, UART, PWM are readily available via a 70 pin board to board connector. This low power Computer on Module is easily found on the market and we decided to use it as the core of our custom platform.

Figure 1: Intel Edison.

Figure 1 shows the tiny processor. Its x86 architecture brings lot of benefits to the embedded controller, which becomes in all respects a custom, low cost, low power and easy to use PC.

Main Features

Figure 2 shows a block diagram resuming the key features of this custom hardware platform. The SPES control system is an Ethernet based distributed network and implements the client-server model foreseen by EPICS architecture. Hence Ethernet connectivity is a key feature of the board. Since Edison Module does not integrate an Ethernet physical layer and neither an Ethernet data link layer we added an Hi-Speed USB 2.0 to 10/100/1000 Gigabit Ethernet controller

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[1] SPES (Selective Production of Exotic Species) is a second generation ISOL radioactive ion beam facility. The aim of SPES is to provide high intensity and high-quality beams of neutron-rich nuclei to perform forefront research in nuclear structure, reaction dynamics and inter-disciplinary fields.

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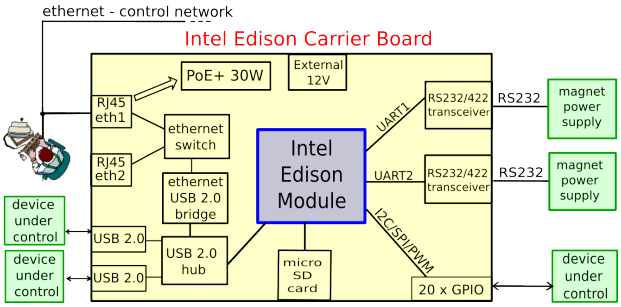

Figure 2: Block diagram.

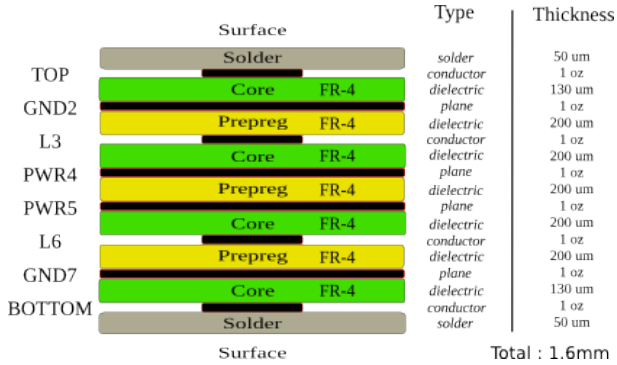

Figure 3: Stack-up.

providing high-performance and cost-effective connectivity solution. Power Over Ethernet (PoE) [4] is a standard for power sourcing devices through Ethernet cabling, up to 30 W (PoE+), that is widely used in IP phones and security cameras. Thanks to the PoE+ capability, this hardware platform can be powered via Ethernet network avoiding to lay cables around the complex and avoiding any modification to the power supply system of devices under control. PoE+ is intended as a 30 W primary DC power source. A secondary power source is provided via a standard 12 V ATX P4 connector. This connector provides a bidirectional DC power way; by powering the carrier via PoE+ the user can extract up to 24 W from the ATX-P4 connector. This is really useful if one needs to power up a non PoE+ device located at the proximity of the Edison carrier board. Furthermore a switch Ethernet ensures the possibility to daisy-chain two Edison carrier boards. Two RS232/RS422 transceivers, directly linked via UART to the processor, have been integrated in the carrier to implement the magnet control system. To minimize the area, no mechanical disk is provided. A flash memory in micro SD form factor is available as a boot device or for logging selected data. A dual stacked type A USB 2.0 connector together with the 20 GPIO header make the system general purpose. An USB hub extends the number of ports available to the processor (Edison provides only one native USB port). Moreover Wi-Fi connectivity makes the custom hardware suitable for applications requiring galvanic isolation.

LAYOUT

The board outline has been set to 132 mm x 72 mm. This small form factor complies with DIN-RAIL mounting, making the embedded controller easy to install on the field. The planning of the Printed Circuit Board (PCB) stack-up took some time and care due to the area and density constraints. A draft of the placement, together with an overview of the distribution of power nets and differential pairs, leaded us to route the PCB on 8 layers as shown in Figure 3. Since there are not special requirements in terms of dielectric, FR-4 glass epoxy has been used (dielectric constant 4.5, loss tangent 0.035). By importing the stack-up in an impedance simulator tool, it is possible to simulate high speed signals requiring a controlled differential impedance.

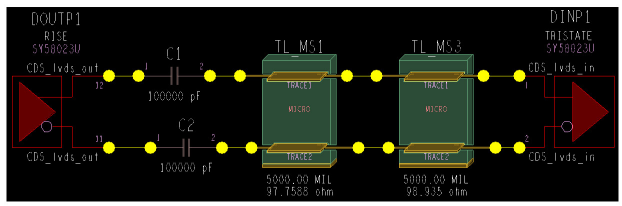

Figure 4: Impedance simulation.

Figure 4 shows a differential pair routed in part on the TOP layer and in part on an inner layer. Stack-up parameters are essential to tune the line width in order to minimize the impedance mismatch seen by the signal crossing the layer change. Importing IBIS models of the driver and receiver stages, provided by manufacturers, together with the proper source or load terminations we could simulate and perform a behavioral validation of the design. Figure 5 depicts the final board layout; only conductor layers are shown. (Top, L3, L6, Bottom). Vias in pad as well as buried vias and blind vias technologies have been avoided.

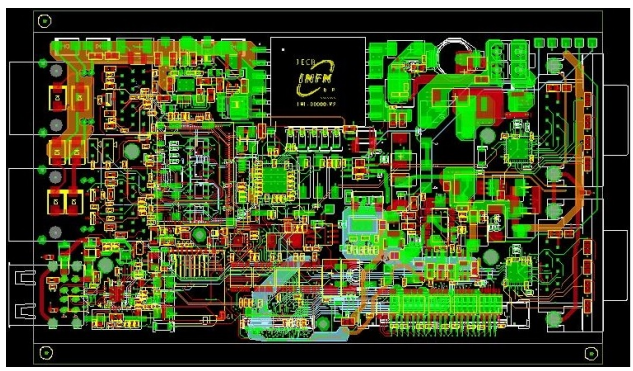

Figure 5: Layout.

Signal and Power Integrity Analysis

Before hardware prototyping we carried out post-layout simulations. This step is crucial in order to foresee signal and power integrity problems [5]. We imported the layout in specialized tools that, by means of full-wave finite element algorithms, are able to compute trace characteristics, discontinuity reflections and cross coupling. Both time and

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frequency domain analysis have been performed on the high speed differential traces. In particular each differential pair has been modeled as a two-port circuit with the related scattering matrix. S-parameters analysis highlights reflections and thus losses due to impedance discontinuities. This analysis is especially useful in multilayer PCB having fragmented reference planes. Afterwards, resonant modes have been investigated. A resonance may lead a net to perform differently from our expectation. Figure 6 shows the areas concerned by natural resonances at 4.8 GHz in the Intel Edison carrier board. The image plots the voltage difference between GND2 and PWR4 planes, where a red color indicates higher voltage amplitude. Since the working frequencies are much below the first resonant mode and are confined in not crucial areas, we decided to tolerate them.

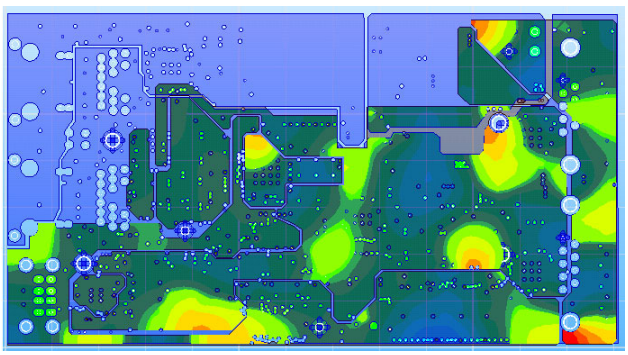

Figure 6: Cavity resonant plot.

Signal and power integrity analysis highlight potentially risky performance due to physical structures on the PCB. However there are also functional problems that may afflict system performance and cannot be included in these analysis. An example follows.

Network Performance

To meet low power requirements and to optimize the thermal profile of the board we used switching regulators and faced noise problems during the debug of the first prototype. We observed poor network performance and dropped packets due to voltage ripple on the 1.2 V power supply of the Ethernet switch's core. A revision of the DC distribution with an improved filtering stage fixed the communication problems. Figure 7 shows the filtered voltage together with the 100 Mbps Ethernet physical layer and the final network test as a proof of the increased data throughput.

SOFTWARE DEVELOPMENT

Intel Edison makes application development straightforward thanks to its full x86 compatibility. Linux or Windows applications can run out of the box without the need to recompile them. By flashing the Edison Module with the latest firmware release (provided by Intel), which is a Yocto [6] complete image, one can bootstrap the target Linux distribution and (by means of "chroot" system call) change the apparent root directory for the current running process to the

Figure 7: Network performance.

chosen Linux distribution. The original image may be replaced with a custom Linux-based system built using Yocto Project tool-set. Another possibility is to make a bootable micro SD card. On the embedded controller we successfully run an EPICS software IOC which loads a database collecting all the local process variables. This fully meets our requirements on the field. The application control GUI is remote in the control room by means of the EPICS client-server access channel structure.

Real Time Peripherals Control

Real time requirements are often met in the control of a particle accelerator. To accommodate this need we have two options in our board: either installing a real time operating system (as Wind River VxWorks for instance) with EPICS support or using the dedicated MCU (microcontroller) integrated in the Edison Module besides the Atom processor. The MCU provides developers with simple and real-time peripheral control capabilities for GPIOs, UARTs, and I2C interfaces further reducing the power consumption. The MCU application runs on the Viper kernel and independently controls the peripherals that connect to the MCU. The microprocessor can communicate with the host Intel Atom processor and wakes it up when needed.

General Purpose I/O - Bit Banging

Twenty digital I/O with selectable voltage level are available on the card and directly mapped to the Edison Module. We used them as I/O pins for digital signals acquisition and as control pins emulating I2C and SPI buses through a simple bit banging technique in python modules.

CONCLUSION

Computer-on-Module approach greatly reduces the development time and costs of embedded systems. The prototype features low consumption (below 3 W with no USB devices attached), and it proved to be an adequate solution for embedding the control of different devices in our accelerator complex: oscilloscopes, magnet power supplies, stepper motors and further appliances accessible via RS232/RS422,

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SPI, I2C, USB, Ethernet. Figure 8 and Figure 9 depict the Intel Edison carrier board.

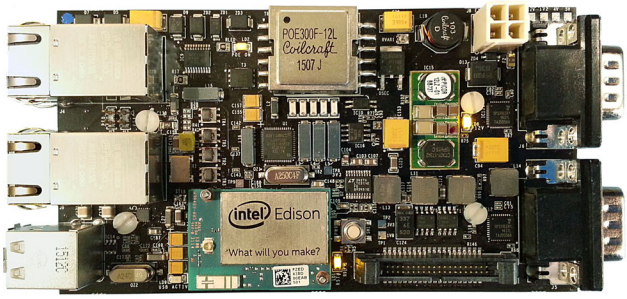

Figure 8: Intel Edison carrier board – top view.

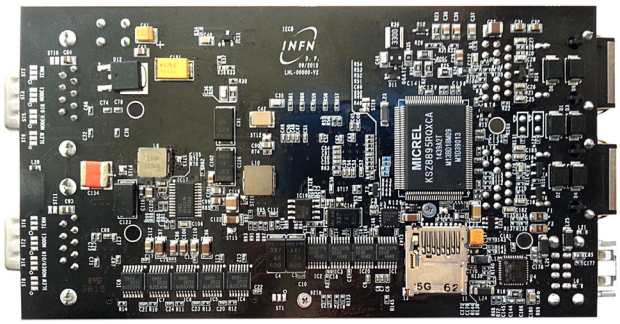

Figure 9: Intel Edison carrier board – bottom view.

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