PERFORMANCE OF THE μTCA DIGITAL FEEDBACK BOARD FOR DRFS TEST AT KEK-STF

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Abstract

The first test of the distributed RF scheme (DRFS) [1] for ILC was carried out at the superconducting (SC) RF test facility in KEK (KEK-STF). The vector sum control for two cavities was carried out by using the μTCA digital feedback board. The compensation for the large-sag owing to the electrical power source and IIR filter, which is also applied as a cavity simulator, was installed. The field stability and performance are reported herein.

INTRODUCTION

An examination of the distributed RF scheme (DRFS) [1] for ILC was carried out at the superconducting RF test facility in KEK (KEK-STF). Two 800 kW klystrons were connected to one RF modulator. Each klystron drove two cavities. The low-level RF (LLRF) system and two klystron units were located in the same tunnel as the superconducting (SC) RF cavities. The vector sum control for the two cavities was performed by using the μTCA digital feedback (FB) board. This board was the same to the one developed for the compact-ERL at KEK [2], but the software was changed for pulse operation. The field stability and the performance are reported herein. The quench detection and detuning effects are summarized in another paper [3].

DIGITAL FEEDBACK BOARD

Figure 1 shows the digital FB boards based on the Advanced Mezzanine Card (AMC) installed in a shelf of μTCA. Two digital FB boards were prepared for the two RF power source. These boards consist of a base card with an FPGA (Vertex5FXT) and daughter cards with four-channel 16-bit ADCs (LTC2208) and DACs (AD9783). The embedded Linux is installed in a PowerPC on the FPGA. Parameter setting or data acquisition is performed through the gigabit Ethernet bus at the backplane. EPICS (Experimental Physics and Industrial Control System) is installed for communication control. Each board plays the role of an EPICS IOC (input output controller). The name of the EPICS records are given as header "uTCA1" or "uTCA2" like a uTCA1:xxxx or uTCA2:xxxx. The labels 1 or 2 in the header are given by a dip-switch on the board. The detail of the digital FB board has been already reported [2].

LLRF SYSTEM

Figure 2 shows the diagram of the LLRF control system. The cavity pick-up signals of 1300 MHz are down-converted to an intermediate frequency (IF) of 10 MHz. The IF is sampled by a 16-bit ADC with 40-MHz.

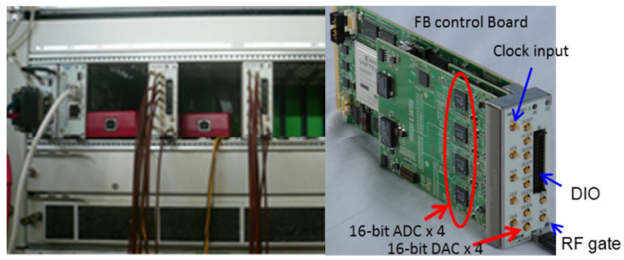

Figure 1: Photograph of μTCA digital feedback board.

Then sampled data are separated to I/Q components. The feedback calculation is performed at 80 MHz in FPGA. The vector sum calculations are performed after the correction of the amplitude and the phase for I/Q. Then, the I/Q data are passed through a digital low-path filter (LPF). The filter is given by the same equation as that of the cavity simulator [4] without detuning, and it is an IIR filter expressed as

$$V_I(n+1) = (1-W)\cdot V_I(n) + W\cdot I(n) \quad (1)$$

$$V_Q(n+1) = (1-W)\cdot V_Q(n) + W\cdot Q(n) \quad (2)$$

where W is the integral of the delay time ΔT and the band width of the angular frequency $\omega_{1/2}$ is given by Eq.(3).

$$W = \Delta T\cdot\omega_{1/2} \quad (3)$$

This IIR filter rejects the noise in the ADC-input and the passband of the TM_{010} mode except for the π mode. When the filter is used as a cavity simulator, the value of $\omega_{1/2}$ depends on the Q_L of the cavity. The cavity simulator is available for a klystron FB or as a test of FB system itself. After passing the IIR filter, the FB calculation of P control is carried out, and the feed-forward (FF) table is added. An amplitude and phase correction for the DAC output is performed. The baseband signals of I and Q from DACs are fed to the IQ modulator, and, then, the 1300-MHz RF signal is fed to the klystron.

The fast interlock system is employed for protection from the arc and reflection as shown in Fig.3. The response time is less than 1 μs. It is the same as the one employed to the machine protection system (MPS) in J-PARC [5].

SAG CONPENSATION

The DRFS modulator has a large sag (~5%) during the modulation of the RF-pulse, and the modulation-anode voltage of the klystron is dull around the leading-edge. For the constant RF-input, the klystron output changed ~10% in amplitude and 40° in phase for the RF-pulse-width of 1.6 ms.

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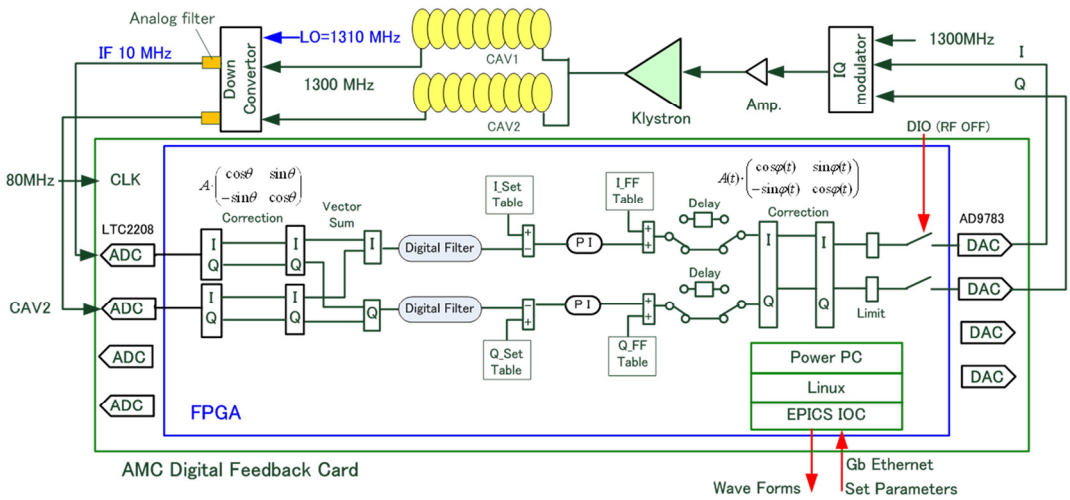

Figure 2: Schematic diagram of the LLRF control system

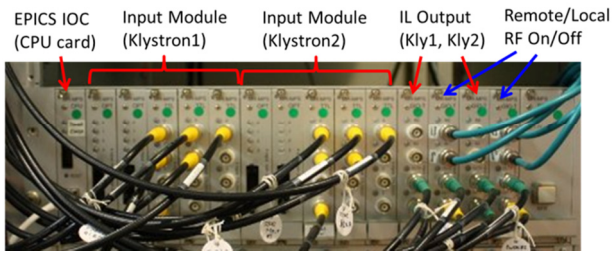

Figure 3: Fast interlock system.

This phase rotation is too large to compensate by using FB only. Hence, the amplitude and phase correction tables are prepared to compensate for the large sag before the DAC-output as shown in Fig.4.

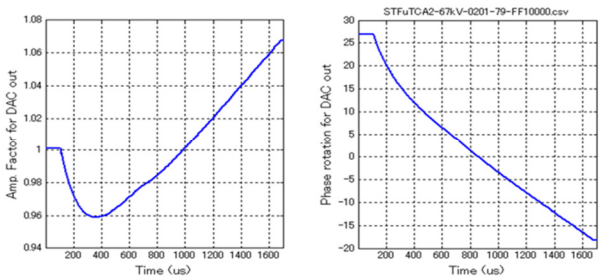

Figure 4: Correction factors for amplitude and phase for the sag-compensation.

GAIN SCAN

As the proportional gain was changed, the stability at the flat-top region was measured. In this measurement, the FB operation was carried out for only one cavity and the IIR filter worked as a 150-kHz LPF. The result of the gain scan is shown in Fig.5. The stability of the amplitude is better around 110 to 160 for the FB gain. Meanwhile, the phase is stable around 60 to 90.

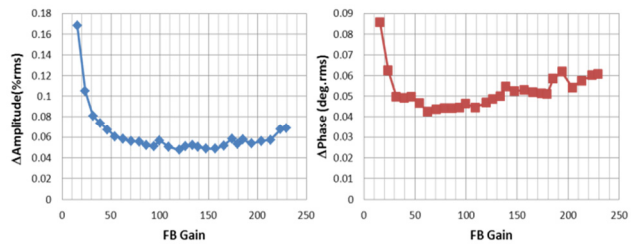

Figure 5: Stability of amplitude and phase for FB gain.

STABILITY AT FLAT-TOP

Figure 6 shows the result of the flat-top region in the FB+FF operation. The vector sum is smoother than the result of each cavity because of passing through the 35 kHz LPF. In the case of FB only, the FB-gain was 97, and the stabilities were 0.06% rms in amplitude and 0.04% in phase. Meanwhile, in the FB+FF operation, the flatness improved. The FF table [6] is based on the DAC output of the FB operation. The stabilities were 0.02 % rms in amplitude and 0.03° rms in phase. These results satisfy the requirement of ILC, i.e., 0.07% and 0.24°.

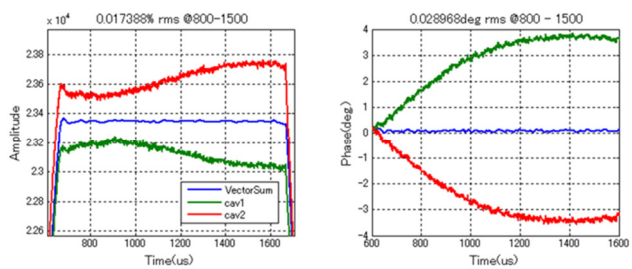

Figure 6: Result of amplitude and phase around flattop region in FB+FF operation. (0.02% rms, 0.03° rms)

LOOP-DELAY SCAN

The cavity is operated in the π-mode. However, in the FB operation without a filter to reject other modes, the RF instability depends on the loop delay due to the

passband of the TM_{010} mode except for the π-mode [7]. In the case of the 8/9π–mode, the phase is 180° different from the π-mode in the cavity pick-up at the 9th cell. The central clearance between the stable region corresponds to the cycle of $1/(f_\pi - f_{8/9\pi})$. By using these conditions, the loop delay is deduced. In order to measure the pattern of stable and unstable operation, the IIR filter was turn off, the digital delay was added in FPGA, and each FB operation was carried out for one SC cavity. Table 1 shows the frequency difference between the π-mode and the other modes measured at each SC cavity. The FB gain in μTCA1 and μTCA2 was about 6 for both.

Figure 7 shows a waveform and a frequency spectrum in the unstable case. The 8/9π-mode was observed, but the 7/9π-mode did not appear because of the filters at the downstream of down-converter; LPF(11 MHz) × 1 and BPF (9.5 MHz – 11.5 MHz) × 3 for μTCA1, BPF× 2 for μTCA2.

Figure 8 shows the intensities of the 8/9π-mode for each additional digital delay. The pattern of stable and unstable operation at the point of the zero digital delay is different between μTCA1 and μTCA2. The FB loop delay at the digital delay that equals zero is deduced as 1.62 μs for μTCA1 and 1.26 μs for μTCA2. The loop delay of μTCA1 is longer than μTCA2 by 0.36 μs. The amount of the difference is broadly explained by the difference of the cable length, ~0.17 μs, and the group delay of BPF, ~0.156 μs. The result of the loop delay is almost the same as the previous one of 1.22 μs, using the cPCI FB system.

Table 1: Frequency differences of TM_{010} passband from π-mode. (Data measured using a network analyser)

mode	**μTCA1** (C2cavity) ***Δf* (MHz)**	**μTCA2** (A2cavity) ***Δf* (MHz)**
π	0	0
8/9π	-0.794	-0.85165
7/9π	-3.06832	-3.2688
6/9π	-6.54258	-6.95866
5/9π	-10.7539	-11.3986
4/9π	-15.1744	-16.1303
3/9π	-19.3084	-20.5185
2/9π	-22.6814	-24.0826
1/9π	-24.9263	-26.3082

SUMMARY

The examination of DRFS for ILC was carried out at KEK-STF. The vector sum operation for the two SC cavities is carried out by using μTCA-digital feedback system. The IIR filter that rejects other modes and the large-sag compensation due to the modulator were performed. Hence, the vector-sum performance satisfied the requirements of ILC.

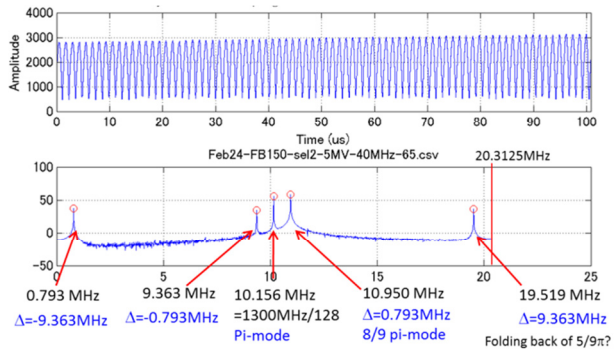

Figure 7: Electric field in the flat-top region (up) and its frequency spectrum (down) in μTCA1 in the case of unstable operation.

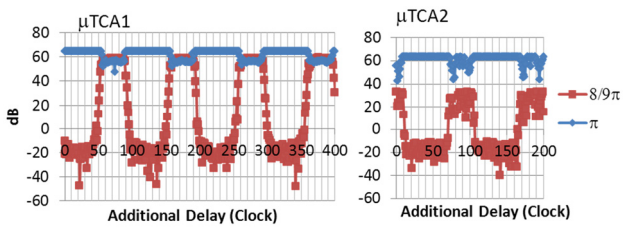

Figure 8: Intensities of the 8/9π-mode for each digital delay (left : μTCA1, right : μTCA2).

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