A DIGITAL POWER SUPPLY CONTROL MODE IN HEAVY-ION ACCELERATOR BASED ON DUAL NIOS CORES*

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Abstract

According to the features of digital power supply and the requirements of pulse mode, this paper introduces a Digital Power Supply Control Mode (DPSCM) in Heavy-Ion Accelerator based on dual Nios cores, which meets the requirements of two basic running modes. The new method develops a system on-chip based on dual Nios cores by using SOPC technology in the Altera EP2C70 FPGA. Compared with traditional DPSCM, the dual Nios cores run simultaneously and cooperate well. As a result, the efficiency of the system is remarkably improved. Cores in parallel can realize reference waveforms switch in pulse mode effectively. We choose an 1150A/185V power supply as test bench. The Experimental result indicates that the system can realize the function of pulse mode, and the stability and tracking error meet the design requirements.

BRIEF INTRODUCTION

DC and pulse are the basic running modes of magnet power supply in Heavy-Ion Accelerator. Ordinary analog magnet power supply with a multilevel data transmission and Digital to Analog Converter can run in DC or pulse mode.

With the development of modern accelerator technology, the output of power supply is required to be more stable and reliable, while the distinguish ability of output and measurement accuracy of tracking error should be higher. Apart from this, people call for the power supply should be easily switched among kinds of running modes, and among kinds of electric current waveforms. At the same time, the need of high-speed remote communication and friendly man-machine interface has been gradually increased. The analog power supply can't meet these requirements, but the digital one has the great advantage in that, which can improve the performance and efficiency of the whole accelerator system.

However, most of digital power supplies run in DC mode. In view of the features of digital pulse power supply, this paper introduces a Digital Power Supply Control Mode (DPSCM) in Heavy-Ion Accelerator based on dual Nios cores, which meets the requirements of two basic running modes.

DIGITAL PULSE POWER SUPPLY

When a digital power supply works in pulse mode, it should output electric current as the reference waveform in Figure 1. And it should output the reference waveform in one time or continuously, and switch among any reference waveforms. In order to cut down the amount of transferring data, the reference waveform usually has a large interval, which is transferred from a remote computer to the control board of digital power supply. So before outputting, this waveform needs to be changed into a waveform with small interval by interpolating. At the same time, the digital power supply regulator need to constantly update reference of electric current during the time of pulse mode. In a word, data transmission, data interpolating or updating reference current value, all of these operations need to monopolize the CPU time. Therefore, ordinary digital power control mode cannot meet the requirements of pulse mode.

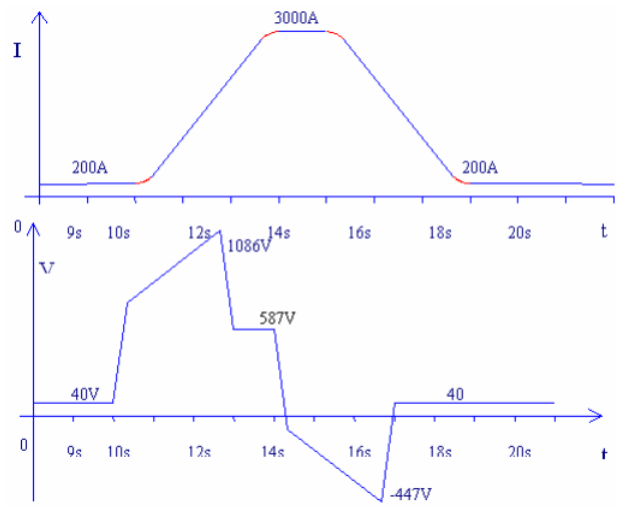

Figure 1: One kind of the current and voltage waveforms when a power supply in heavy-ion accelerator works in the pulse mode.

SOPC BASED ON NIOS II PROCESSOR

Features of Nios II processor

Nios II processor is a user-configurable 32-bit RISC soft-core processor developed by Altera. In order to meet the requirements of performance and price, its features and peripherals can be added or cut down as need. And it plays an important role in SOPC (System on a Programmable Chip) technology.

People can create or debug a system with multiple Nios II processors. With many good features provided by Altera, such as Avalon Bus Switches and multiple master-

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slave ports, the Nios II system has a good ability of bus arbitration. What's more, multiple Nios II processors in a system can efficiently share resources.

Development Environment

SOPC Builder is an automated SOPC development tool, integrated within the Quartus II software, which enables users to define and generate a complete SOPC in much less time than using traditional manual design method. SOPC Builder modules are the building blocks for creating an SOPC Builder system. SOPC Builder modules use Avalon interfaces, such as memory-mapped, streaming, and IRQ, for the physical connection of components. People can use SOPC Builder to connect any logical device (either on-chip or off-chip) that has an Avalon interface.

Custom Components

Users can import HDL modules and entities that users write in Verilog HDL or VHDL into SOPC builder as custom components. When it comes to digital power supply, the most important custom component is the digital power supply regulator, which does digital PI operations and generates PWM signals. If the program of the digital power supply regulator meets the requirements of Avalon Bus, people would change the reference electric current value or parameters of regulator by writing the registers through Avalon Bus.

DPSCM BASED ON DUAL NIOS CORES

Hardware Design

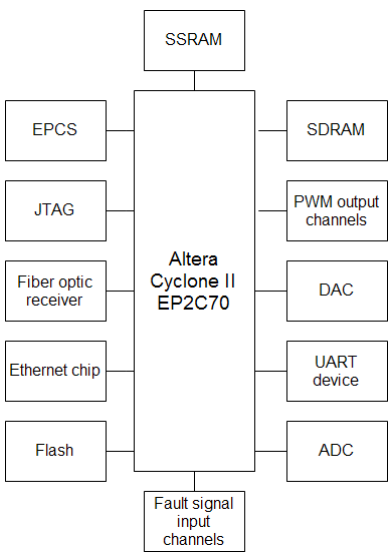

Figure 2: Hardware block diagram

The hardware of DPSCM based on dual Nios cores includes Altera EP2C70 FPGA and peripherals including Ethernet chip, fiber optic receiver, Flash, SDRAM, SSRAM, EPCS, UART device, ADC module, DAC module, PWM output channels and fault signal input channels. All peripherals connect with the pins of Altera EP2C70 FPGA. Figure 2 shows the hardware block diagram of digital power supply based on EP2C70.

SOPC

The Digital Power Supply Control Mode (DPSCM) in accelerator based on dual Nios cores, is a kind of SOPC based on Altera FPGA device.

According to Figure 3, the system structure of DPSCM based on dual Nios cores can be divided into 3 domains: domain of communication, domain of share and domain of regulator.

Domain of communication includes Nios II CPU, Ethernet controller, synchronous optical fiber component, Timer, Watch Dog, JTAG UART, PLL and UART. Domain of regulator includes Nios II CPU, Timer, and Watch Dog. Domain of share includes an EPCS controller, Flash controller, SDRAM controller, SSRAM controller and digital power supply regulator. In a domain, all of controllers are connected to the corresponding Nios II CPU by Avalon Bus.

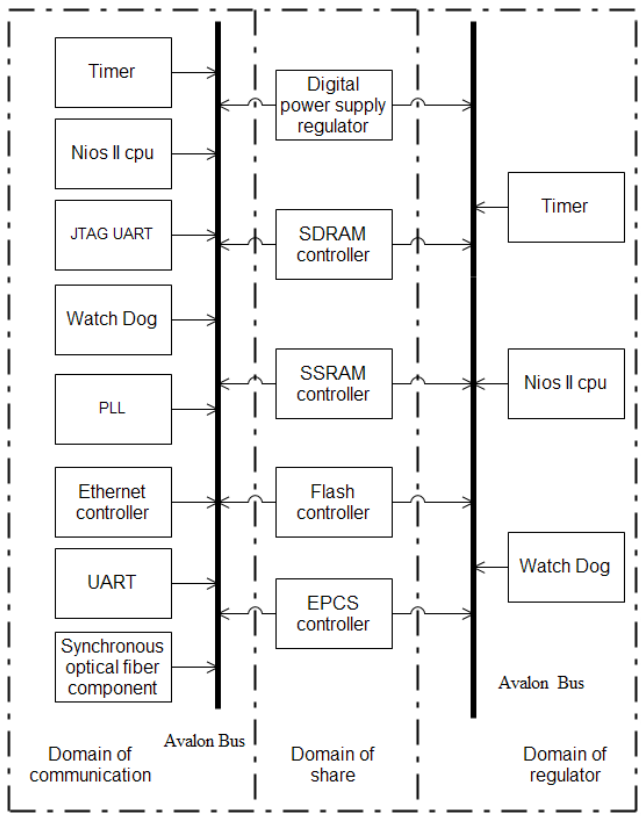

Figure 3: The structures of SOPC

Software Design

Two Nios II processors can be programmed by Nios II Software Build Tools after the SOPC mentioned above has been created. Only connected to the CPU by Avalon Bus can the module be controlled by the CPU. So domain of communication mainly communicates with peripheral devices. It communicates with debug interface by serial port, or with remote computer by Ethernet, or with sync

system by optical fiber. In addition, it configures parameters of digital power supply regulator and does waveform interpolation. Domain of communication has been transplanted of μC / OS II because of its complicated functions.

Domain of regulator also configures parameters of digital power supply regulator, but its main function is updating the reference of electric current.

Domain of communication and domain of regulator share the memories. And the SDRAM is the major shared memory. SDRAM is adopted the method of static storage. It means that SDRAM has been divided into many data areas and flag bits. Two Nios II CPUs in the domains query the flag bits to know whether there are any events. So the two cores can communicate with each other and exchange data.

To sum up, Communication and data processing is completed by one Nios II CPU and reference current setting is completed by the other. Compared with traditional DPSCM, the dual Nios cores run simultaneously and cooperate well, and the efficiency of system is remarkably improved, further, cores in parallel can realize reference waveforms switch in pulse mode effectively.

DEBUG

We choose an 1150A/185V digital power supply based on dual Nios cores for dipole magnet as test bench to do many experiments. This power supply has been used in accelerator experiment since 2010, and worked for more than 3 months per year. The requirements of DC and pulse mode are satisfied, while it triggers the output waveform either in one time or continuously, and can switch among 256 reference waveforms without delay.

The performance of this power supply has significantly been improved because of its fully digital control method. We easily pick up kinds of debug data from the power supply, such as sampling value of output current, output value of regulator, tracking error of current and so on. With these data, we can do data analysis to guide modifying the parameters or the structure of regulator.

Figure 4 shows the reference current and tracking error. The data is uploaded to a PC from the digital power supply by serial port or Ethernet. Refer to Figure 4, the abscissa is the sample point, and the y-axis is normalization current. The interval of two neighbor simple points is 16us. When normalization current is 1, the true current value is 2000A (maximum input of DCCT). We can draw a conclusion tracking error on rising stage of pulse is less than $\pm 1.0\times10^{-4}$, that on top stage is less than $\pm 1.0\times10^{-5}$.

Figure 5 shows the ripple current of the power supply. This figure is from data analysis of sampling value of output current. Refer to Figure 5, the abscissa is time (s), and the y-axis is the ripple current (A). The data is acquired when the output current is 50A. As a result, the relative ripple current when on bottom stage is less than $\pm 1.0\times10^{-4}$.

CONCLUSION

- The digital power supply based on dual Nios cores is an all-digital pulse power supply.
- Compared with other power supplies, the digital power supply based on dual Nios cores saves hardware cost.
- With new concept of SOPC, the digital power supply not only improves the performance, but also meets the real-time requirement of pulse power supply.
- Uploading debug data by digital interface provides a new concept for future designing and debugging digital power supplies.

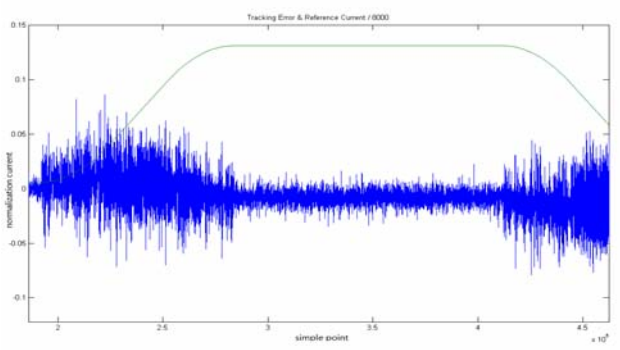

Figure 4: Reference current and tracking error.

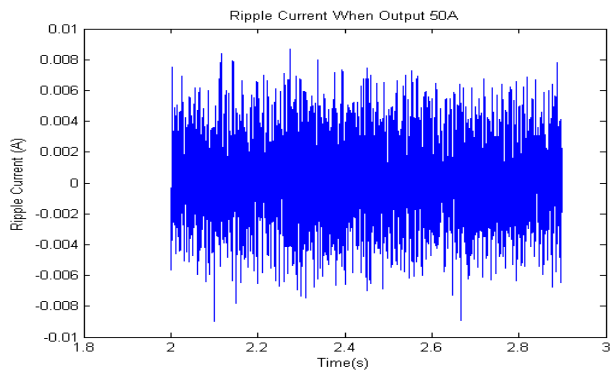

Figure 5: Ripple current.

REFERENCES

[1] Huang Yu-Zhen. Research and Design of Digital Power Supply Regulator Based on FPGA. Doctoral dissertation, GUCAS, 2010.

[2] Altera Corporation. SOPC Builder User Guide. [M]December 2010. http://www.altera.com.

[3] Altera Corporation. Nios II Processor Reference Handbook. [M]October. 2007. http://www.altera.com.

[4] Altera Corporation. Creating Multiprocessor Nios II Systems Tutorial. [M]February, 2010. http://www.altera.com.