A FAST 650V CHOPPER DRIVER

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Abstract

In the framework of Linac4 and the Superconducting Proton Linac (SPL) studies at CERN, the design for a beam chopper has been carried out]3_. The chopper is basically a kicker that deviates part of the beam towards a dump. It is made of two 50 Ω, slow wave lines facing each other, matching the beam velocity and driven with a minimum of 500 V. Due to the bunch spacing of 2.84 ns, a system rise and fall time (3 %-90 %) below 2.5 ns is required with pulse lengths ranging from 8 ns to hundreds of μs. Although different solutions for the driver amplifier where devised in the past, none of the achievements was entirely satisfactory. This paper describes a new design and prototype that meets all the required specifications.

INTRODUCTION

The chopper foreseen in the medium energy line of the Linac4 and SPL is basically a kicker that deviates part of the beam towards a dump. It is made of two 50 Ω, slow wave lines facing each other, matching the beam velocity and driven with opposite polarity signals. Simulations have shown that to divert the beam towards the dump, the slow wave lines should be driven with ±500 V. A voltage above 600 V will then leave a sufficient security margin.

The residual field experienced by the accelerated beam must stay below 3 % of the extraction field so that, with a bunch spacing of 2.84 ns, a 3 %-90% system rise and fall time below 2.5 ns is required (including jitters and other imperfections). For maximum flexibility, the system must be able to remove any number of consecutive bunches with a minimum of 3 and up to a few thousand. Therefore driving pulse lengths ranging from 8 ns to hundreds of μs and repetition rates as high as 45 MHz are required.

DESIGN CONSIDERATIONS

Available devices

The most suitable devices for this application are MOSFETs. These components can handle high voltage, high current and also be very fast but none of those presently on the market satisfy our entire requirement. As switching time is the only characteristic that cannot be achieved else than by the device itself, a parallel/series combination of lower voltage and current devices must be used.

Stacking configuration

Paralleling MOSFETs is common practice for increasing the available current and power and does not present particular difficulties. However, connecting them in series to handle voltages higher than rated for a single device requires special attention. If the MOSFETs series stack has to be supplied from a single voltage source,

precautions must be taken to guarantee equal voltage sharing and not exceeding the maximum rating. This is a difficult task because even in case of minor problems, such as a slight drive synchronization error can result in severe device overvoltage and the loss of the entire MOSFET stack.

An intrinsically safe, multi-stage configuration that allows building up high output voltages from lower voltage units exists provided each unit is floating and can be individually supplied. The basic circuit is shown in fig.1. The energy being transferred to the load (R) is stored in the capacitors (C). All capacitors are charged at the same voltage and floating. When the MOSFETs (Q) turn-on, the capacitors become series connected and discharge into the load which will see the sum of the individual capacitors voltage. Each stage has to supply the full load current and thus sees an equivalent load R/N.

In case of timing errors among the modules switching or also if some MOSFET will not turn-on at all, a current path will always exists through diodes (D) so that the output voltage will simply be reduced by the contribution of the missing stage.

If for any reason the voltage across a diode D rises above the capacitor voltage, the MOSFET reverse diode will turn-on and automatically prevent over voltage across the MOSFETs.

As the circuit is completely floating, either point *OUT+* or *OUT-* may be grounded to invert the output signal polarity. Of course in reality each stage will have some leakage capacitance whose effects at high frequency must be controlled to achieve the required switching speed.
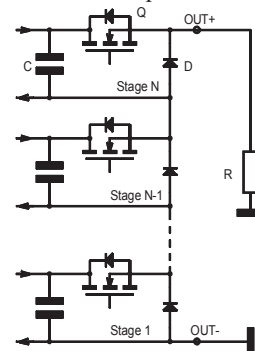
Figure 1: Stacking configuration

Supplying the power

In pulsed operation, supplying the required energy to the capacitors while maintaining them floating can be achieved as shown in fig. 2. With the switch *SW* in charging position V_{SUPPLY} charges all the capacitors in parallel through the diodes D_A and D_B. Opening *SW* will reversely bias D_A and D_B thus isolating each stage from the others. Low reverse capacitance diodes must be used. Note that V_{SWITCH} must be higher than the maximum

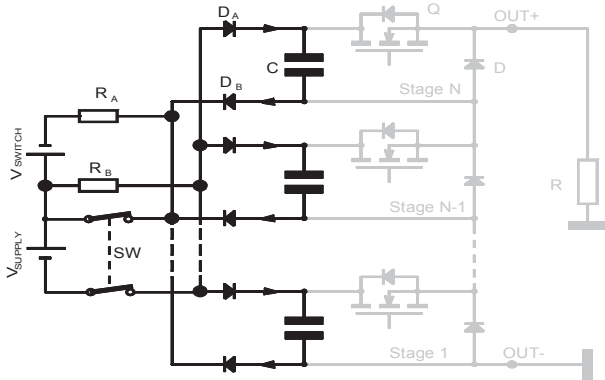output voltage to ensure reverse diode bias conditions for all the stages.

Figure 2: Supply configuration.

Gate drivers and MOSFET selection

The choice of the power device and the gate driver is strictly linked because the ensemble must satisfy the rise/fall time and voltage specifications but also the requirements in terms of jitter and thermal stability. There is no need for the pulse amplifier to be linear.

Isolating the driving signals

While building-up the output pulse, each stage will rise to a voltage level corresponding to its position in the stack. Therefore the common input control pulse has to be independently applied to each stage through an individual level shifter/isolator.

BASIC MODULE

The basic module (fig.3 and 4) is built around Freescale RF MOSFETs type MRF6V2010N. This is a high speed device that typically withstands 110 V, has a saturation current above 1.5 A, very limited internal capacitances (C_i~17 pF, C_o~8 pF and C_r~0.13 pF) and low threshold voltage (~2 V). The standard logic family best suited as gate driver in this application is AC/ACT one. Its internal output stage configuration based on symmetric MOSFETs allows parallel connection of the outputs, guarantees high peak switching current, high frequency operation and rapid pulse fronts. With these two components switching time of about 1 ns can be achieved.

Six MRF6V2010N are connected in parallel on a 10 Ω characteristic impedance strip-line. Ferrite cores limit the leakage capacitance effect on the load at high frequency. Two such modules are connected facing each other so that at the centre the characteristic impedance halves to 5 Ω.
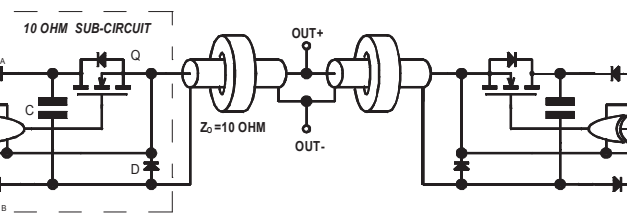
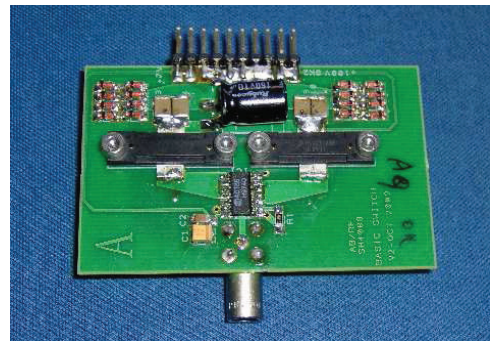The voltage achievable from this module is ~80 V.

Figure 3: Basic module.

Figure 4: 10 Ω sub-circuit card.

POWER AND CONTROL PULSE ISOLATOR

Generation of the floating driving pulses from the common input signal is done by the circuit shown in fig.5.

A common amplifier drives in parallel ten pulse transformers (one for each of the required stages). The transformer provides galvanic isolation has two counter-phase outputs and is arranged such to minimize the capacitance between input and floating outputs. Each output signal is derived using a high-pass filter to obtain short pulses corresponding to the rising and falling fronts of the input signal. A flip-flop is then set and reset by these pulses to reconstruct the original driving signal. Individual adjustment of the rising and falling fronts delay allows exact synchronization.

To achieve the speed and time stability requirements, ECL logic is used to reconstruct the driving pulse. The circuit also provides the floating supply required by the gate drivers. It uses commercial 2 W isolated DC-DC converters with only 2 pF capacitance between input and output.
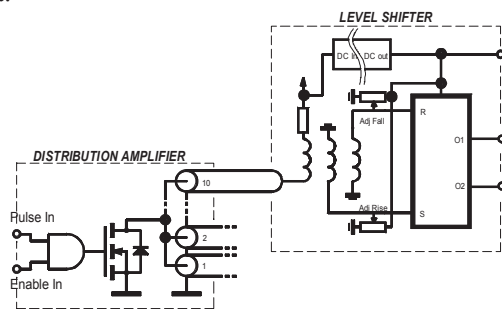

Figure 5: Power and control pulse isolation.

PULSER ENSEMBLE

The pulse amplifier is housed in a 19", 6 units high and 730 mm long rack mount chassis. Ten 5 Ω modules are mounted in the box that also contains the level shifters, the power supplies and protection interlocks (Fig.6).

The 10 Ω characteristic impedance strip-lines are made with thin and flexible printed circuit material. They are mechanically and electrically stacked at their center where the signals are summed-up. Each level shifter card drives in parallel the two 10 Ω sub-circuits used in a 5 Ω module. High frequency common-mode isolation is implemented using ferrite cores. They surround each

strip-line, the connections between the level shifter cards and the 10 Ω sub-circuits as well as the output cable.
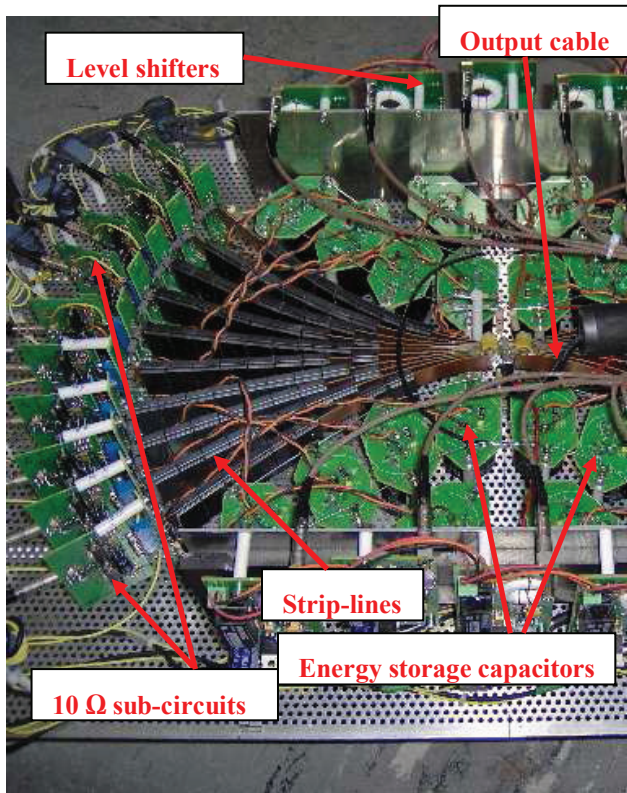

Figure 6: Amplifier layout (half).

Ancillary circuitry takes care of power supplies turn-on sequencing, timing control, protections as well as remote ON/OFF control and status acquisition. Although each individual 10 Ω sub-circuit can be safely operated on an open or short circuit, a load status interlock enables the pulse amplifier only with load resistance of 25 Ω÷100 Ω.

The input control pulses are transferred to the output during a time window (2 ms max) started by a dedicated trigger pulse.

MEASURED PERFORMANCES

The pulse amplifier has been fully characterized on a 50 Ω attenuator. Measurements have been done for both output polarities obtaining almost identical results. Polarity switching is extremely easy as one only needs to invert the output cable connection.

The pulse output voltage along the burst varies from a minimum of 650 V to 700 V. This value could be easily increased by 50 V. The measurements have been done at 2 Hz burst repetition frequency. Increasing it to 50 Hz would bring the power dissipation per device to ~2 W and could be easily handled with adequate air cooling.

The maximum pulse length (100 μs) can probably be extended to cover the whole burst length (2 ms).

The pulse length distortion and input-output delay are limited to 300 ps but they are not constant. The first is proportional to the pulse length while the latter increases along the burst and with frequency.

07 Accelerator Technology

T30 Subsystems, Technology and Components, Other

The following table summarizes the achieved performances and the following plots show measured signals.

Table 1: Main pulse amplifier parameters

| Parameter	Value
Output voltage (V_{max})	≥650 V
Load impedance	50 Ω
Pulse frequency	≥45 MHz
Burst length	1 ms
Burst repetition frequency	2 Hz[†]
10%-90% rise and fall time	1.5 ns typically
3% - 90% rise and fall time	≤2.5 ns
Minimum pulse length	≤8.0 ns
Minimum off time pulse	≤10.0 ns
Maximum pulse length	100 μs[†]
Residual voltage between pulses	≤3% of V_{max}
Pulse length distortion variation	≤300 ps
Input output delay variation	≤300 ps

† see text
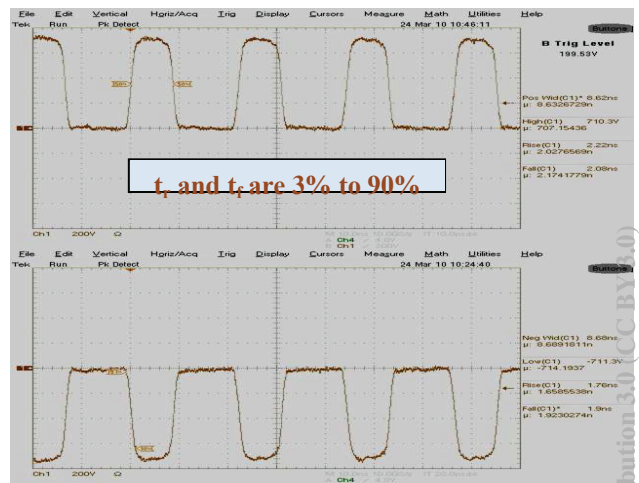
Figure 7: 45MHz, 8.6ns positive and negative pulses [10ns/div – 200V/div]

CONCLUSIONS

The stringent requirements of the CERN Linac4 and SPL chopper driver are fulfilled by this design. In particular the output voltage, rise and fall times as well as delay and pulse distortion stability are compatible with the foreseen use.

The design is based on standard components readily available on the market and its modular construction permits easy testing of all parts.

The possibility of reversing the output signal polarity is also a very important feature.

REFERENCES

]1_F. Caspers, T. Kroyer, M. Paoluzzi, "Cern chopper final report", AB-Note-2008-040 RF, CERN, Geneva, 2008