DEVELOPMENT OF A DIGITAL LOW-LEVEL RF CONTROL SYSTEM FOR THE p-LINAC TEST STAND AT FAIR*

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Abstract

A test stand for a proton Linac is currently being built at GSI in the context of the FAIR project. Its low-level rf control system will be based on a system that has been developed for the S-DALINAC at TU Darmstadt operating at 3 GHz. This system converts the rf signal coming from the cavity down to the base-band using a hardware I/Q demodulator. The base-band signals are digitized by ADCs and fed into an FPGA executing the control algorithm. The resulting signals are I/Q modulated before they are sent back to the cavity.

The rf module has to be adapted to the p-LINAC's operating frequency of 325 MHz. Moreover, the p-LINAC will run in pulsed operation whereas the S-DALINAC is operated in cw mode. Different characteristics of the cavities and the pulsed operation require a redesign of the control algorithm.

We will report on the modifications necessary to adapt the S-DALINAC's control system to the p-LINAC test stand and on first results obtained from tests with a prototype.

INTRODUCTION

A significant part of the experiments at the Facility for Antiproton and Ion Research (FAIR), currently under construction at GSI in Darmstadt, Germany, is dedicated to antiproton physics. The production of a high-intensity antiproton beam demands for an initial proton beam current of up to 70 mA at a beam energy of 70 MeV. As these parameters exceed the limits of the existing UNILAC accelerator, a new p-Linac is under development [1].

This normal conducting drift tube linac comprises 12 crossed-bar H-mode cavities (CH cavities) that are operated at 325.224 MHz in pulsed mode [2]. The cavities are coupled pairwise via coupling cells. This allows to feed two cavities with a single klystron. The power coupler is located in the coupling cell.

The cavities are fed with rf pulses of $\leq 200\,\mu$s length at a maximum repetition rate of 4 Hz [3]. The beam pulse length is 36 μs. During this time additional rf power is needed to maintain a stable field. The target specification for the relative amplitude error is 10^{-3} rms.

The low-level rf control system for the p-Linac is based on a system that has been developed for the Superconducting Darmstadt Electron Linear Accelerator (S-DALINAC) at TU Darmstadt. For a detailed description of this system see [4]. In the following we will describe the architecture of the system and modifications that are necessary to adapt this system to the demands of the p-Linac at FAIR.

HARDWARE

The in-house developed rf control system follows the base-band approach. This allows to split the hardware into two parts: A frequency-dependent rf board containing the quadrature (de)modulator and a frequency independent FPGA board processing the signals. An overview of the hardware is shown in Fig. 1.

RF Board

The operating frequency of the p-Linac cavities of 325 MHz is much lower than the operating frequency of the S-DALINAC of 3 GHz. Thus the rf board had to be adapted to the new frequency. A slightly modified revision of an rf board designed for the S-DALINAC has been described in [5]. Since the demodulator of that board did not provide satisfying results, a new revision has been designed and produced. The modifications compared to the S-DALINAC boards comprise the replacement of the quadrature (de)modulator and directional couplers with appropriate components for 325 MHz as well as a complete redesign of the printed circuit board. In contrast to the first version of the board, the demodulator and modulator components use a local oscillator frequency of twice the carrier frequency to derive the two internal carrier signals for I and Q. This solution was checked to provide sufficient accuracy for frequencies as low as 325 MHz.

A separate rf power detector improves the accuracy of the magnitude measurement. This feature had been implemented to achieve the high amplitude accuracy needed at the S-DALINAC, but it has been maintained for the p-Linac rf board, too. The availability of a separate amplitude detector allows to use the quadrature demodulator solely to detect the phase of the input signal.

Before analog (de)modulator circuits can be used for precision measurements, a careful calibration has to be done individually, the details of which have been described in [4]. However, not all errors of the (de)modulator can be compensated by calibration. An important figure of merit of the demodulator is the deviation of the measured input phase from the actual input phase. This has been measured by applying an rf input signal to the rf board with a frequency that is slightly shifted to the LO frequency (1 kHz away). The result is a rotating vector in the I/Q plane

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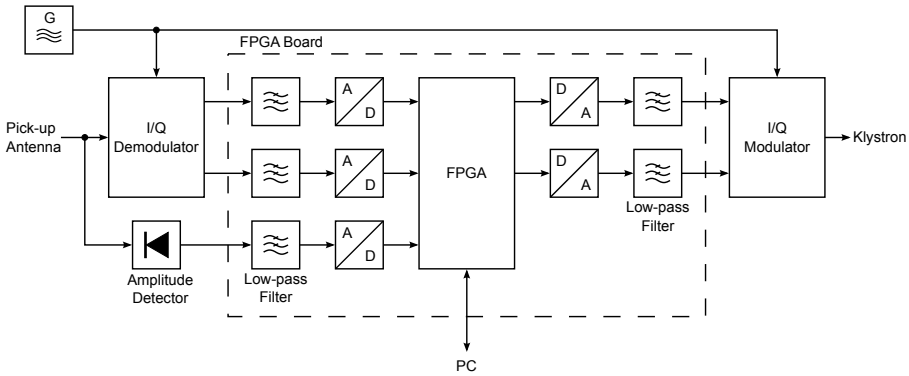

Figure 1: Overview of the hardware components of the rf control system. Modulator and demodulator are located on the rf board whereas the FPGA board contains the signal processing hardware.

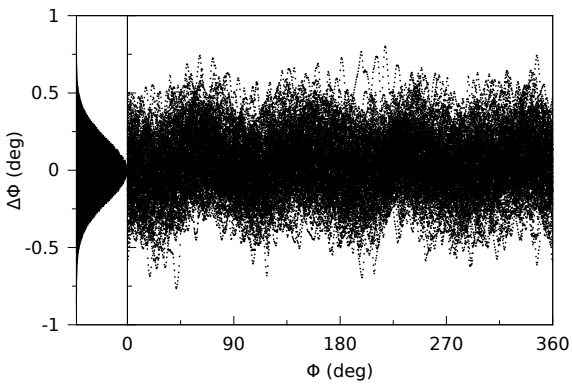

Figure 2: Typical deviation of the measured input phase from the actual input phase plotted vs. the actual input phase. The histogram on the left shows a projection to the y axis with a root square deviation of the distribution of $\Delta\phi_{\mathrm{rms}} = 0.2°$. The data has been acquired over ≈ 0.1 s.

that is recorded over many periods. Fitting the I and Q components with $A_I \cos(\omega t + \phi_I)$ and $A_Q \sin(\omega t + \phi_Q)$, respectively, provides a good approximation of the actual input signal. Figure 2 shows the deviation of the phase calculated from I and Q and the input phase obtained by the fit. The phase error is dominated by noise, partly produced by the two rf generators. With $\Delta\phi_{\mathrm{rms}} = 0.2°$ the root square deviation is smaller than the phase error of the 3 GHz boards currently used at the S-DALINAC. The deviation of the phase shift between I and Q from the ideal 90° is 0.17°. All together the described hardware errors are negligible, showing the substantial improvements compared to the boards used before [5].

FPGA Board

The FPGA board digitizes the analog signals coming from the rf board and feeds them into its FPGA where the control algorithm is carried out. The resulting digital I and Q outputs are then reconverted to analog format before they are sent back to the rf board. The FPGA board used at the beginning of the project has been replaced by an improved revision. The hardware of the FPGA board is identical with the boards used at the S-DALINAC except for the filters.

Low-pass filters in front of the ADCs ensure that frequencies above the Nyquist frequency are damped to avoid aliasing effects. Identical reconstruction filters at the output remove harmonics created by the DACs. The filters have been designed for the S-DALINAC's rf control system which has to deal with microphonics below 10 kHz frequency. High requirements with respect to accuracy together with an adjacent mode of the cavity that is only 700 kHz away from the operating frequency led to third-order π filters with an cutoff-frequency of ≈ 100 kHz. On the other hand the phase shift introduced by the filters decreases the gain margin of the controller. That is why the filters have been reduced to first order filters with the same cutoff-frequency for the p-Linac rf control system. These filters still provide enough attenuation for the neighboring mode.

CONTROL ALGORITHM

Two different control algorithms have been implemented for the S-DALINAC: A generator-driven resonator control algorithm for normal-conducting cavities and a self-excited loop algorithm for superconducting cavities [4]. Both algorithms are optimized for cw operation and cannot be used in pulsed mode with the p-Linac. The control algorithm for the p-Linac is an enhanced version of the generator-driven algorithm for the S-DALINAC.

A first revision of the p-Linac control algorithm is shown in Fig. 3. Phase and amplitude are controlled separately. The input phase is calculated from I and Q using the CORDIC algorithm, while the amplitude is measured directly with the power detector on the rf board. The amplitude as well as the phase controller use integral controllers in addition to the proportional controllers to eliminate steady-state offsets that remain after applying proportional control. A differential controller has been foreseen, but is finally used with zero gain as it turned out to amplify the noise solely without contributing to the control accuracy. The output of the amplitude controller and the phase

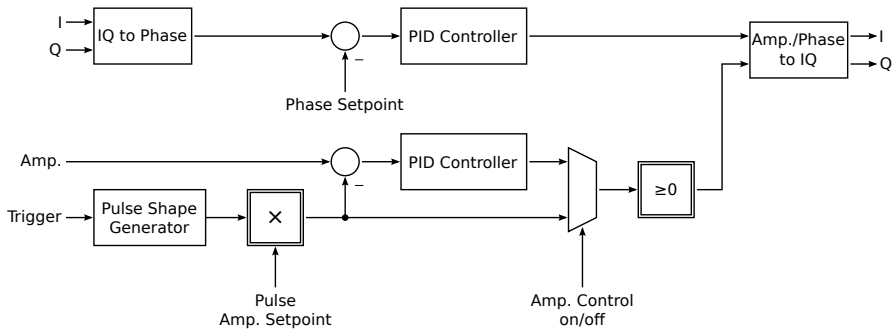

Figure 3: Simplified flow chart of the control algorithm used for first tests.

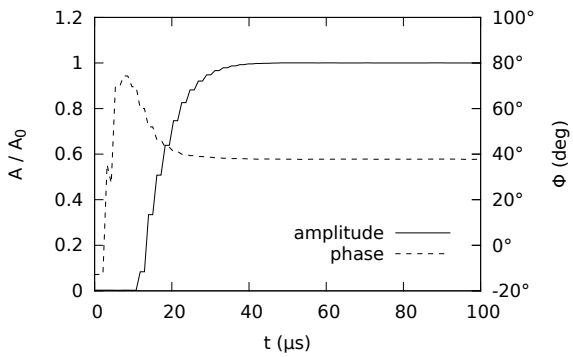

Figure 4: Step response of the closed control loop measured using a test cavity with $Q_L \approx 1000$.

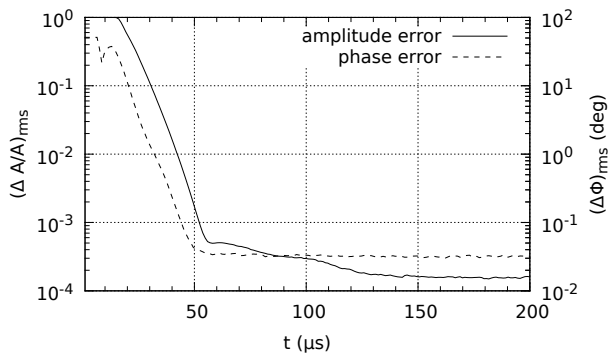

Figure 5: Amplitude and phase error during a 200 μs pulse. The pulse starts at 0 μs when the set value jumps from 0 to the set value.

controller is transformed to I and Q and sent to the rf board.

In contrast to cw operation the set value of the amplitude controller must not be constant, but has to vary periodically to generate pulses. This is accomplished by a pulse shape generator that is implemented in the FPGA. It consists of a memory storing 2048 set values that constitute a pulse shape of up to 2 ms in length. Up to now, the trigger signal for the pulse generator is generated periodically inside the FPGA. At the p-Linac test stand an external trigger signal will be used.

Between pulses the input signal vanishes, and thus the input phase has no meaningful value. To ensure that this does not affect the integral phase controller, its accumulator is set to hold between pulses.

The performance of this control algorithm has been tested by measuring the amplitude and phase errors using a dummy cavity with a loaded quality factor of $Q_L \approx 1000$. Figure 4 shows the step response of the closed loop whereas Fig. 5 shows the rms errors over the time relative to the beginning of the pulse. The rms errors have been calculated from the corresponding errors at the same relative time over a set of 1000 pulses. It takes about 50 μs to stabilize amplitude and phase to the target specification. To achieve a faster response the control algorithm has to provide a feed forward signal which is currently implemented.

SUMMARY

The rf control hardware initially designed for the S-DALINAC has been adapted for the FAIR p-Linac. A new rf board allows operation at 325 MHz, while redesigned filters provide a much faster response of the controller. Until the first cavity arrives at the test stand at GSI, tests of the rf control system are done with an FPGA-based cavity simulator that is currently under development.

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