THE DEVELOPMENT OF LLRF SYSTEM AT PAL *

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Abstract

The Super Conducting Radio Frequency (SCRF) systems will be installed for PLS-II. The PAL has been carrying out the design of the low level radio frequency (LLRF) system for the SCRF control using the digital technologies. The requirements of the LLRF system are to maintain the field stability in a cavity within ±0.75% in amplitude and 0.35° in phase. The LLRF system includes the RF front-end, analog and digital board (ADC, DAC, FPGA, etc.), clock generation and distribution, and so on. The control algorithm will be implemented by the VHDL. The hardware design of the LLRF for PLS-II, simulation and test results were described in the paper.

INTRODUCTION

With the high performance of the digital components such as digital signal processor, field programmable gate array (FPGA), analog to digital converter(ADC) and digital to analog converter(DAC), almost control systems adapt digital technology instead of analog system using the operational amplifier which was popular in 1990s. The improved performance of the FPGA nowadays has been using widely in the system circuits design owing to its high density and flexibility.

The PAL finished the upgrade project as the table 1 that showed major upgraded parameters. The RF systems have been operating with the normal conducting cavity, but they will be replaced with superconducting cavity in near future.

Table 1 : RF relative parameters of the PLS and PLS-II.

Parameters	Unit	PLS	PLS-II
Energy	GeV	2.5	3.0
Current	mA	200	400
Emittance	nmrad	18.9	5.9
RF frequency	MHz	500.082	499.973
Revolution Frequency	MHz	1.068	1.064
Harmonic Number		468	470

Many accelerator laboratories over the world adopted the digital LLRF systems that gave the satisfied stabilities to accelerator operation [1-2]. The LLRF system also provides interlock handling, user interface panel, self-diagnosis, signal capture for faults analysis, and so on.

This paper presented the hardware structure of the LLRF, board design and some simulation results of VHDL functions related to the LLRF signal processing.

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LLRF SYSTEM

The figure 1 shows the PLS-II RF system that consists of the klystron, cavity, LLRF system, RF analog front-end and so on. The RF section includes the 550MHz of local frequency (LO) oscillator, IQ modulator with amplifier and filter, down converter of 50MHz intermediate frequency for RF input signals such as cavity field, forward and reflected signal. For the case of direct digital synthesizer (DDS), up-converter circuits from 50 MHz IF to 500MHz RF also implemented. The Microblaze processor was embedded for the interface between consol and VHDL logic, and direct in-out digital signal control and monitor [3].

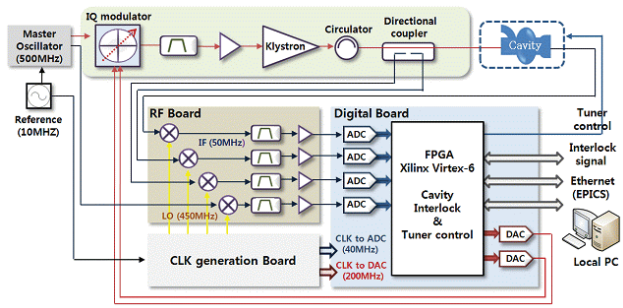

Figure 1: Block diagram of the LLRF system for PLS-II.

The LLRF system was implemented using the Vertex6 FPGA(XC6VLX75T), with four 16-bit ADCs, a DAC which has dual 16-bit channels and a Spartan6 FPGA for clock generation and digital input & output interface as shown in the Fig 2. The Spartan6 was developed to dedicate the clock handing with the low time jitter. The FPGA, XC6VLX75T key component at LLRF, has many features [3].

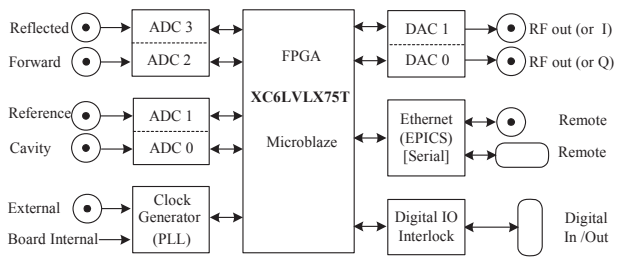

Figure 2 : Block diagram of the designed FPGA with peripheral devices.

It has two ADC daughter boards and each has two ADC channels respectively, thus four ADCs are

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implemented to digitize the RF signals of the forward, reflected, cavity and reference. The LTC2205 from Linear Technology was adapted for the ADC which has 16-bit resolution and 65Msps throughput. With the 500MHz RF signal and 550MHz LO, the IF of LLRF was given for 50MHz. This signal was digitized using the conventional IQ method where the sampling frequency was chosen by the 4/5 ∗ IF = 40MHz. The sampled both I and Q components are regulated by the PI compensator, and are transferred to DAC output to generate the vector-control signal. Figure 3 shows the printed circuits board of the LLRF. The FPGA was on the plane mother board and the other boards like ADC, DAC and clock generation are assembled on the mother board. Thus it makes the test easy and modification of the daughter board also gives cost effective.

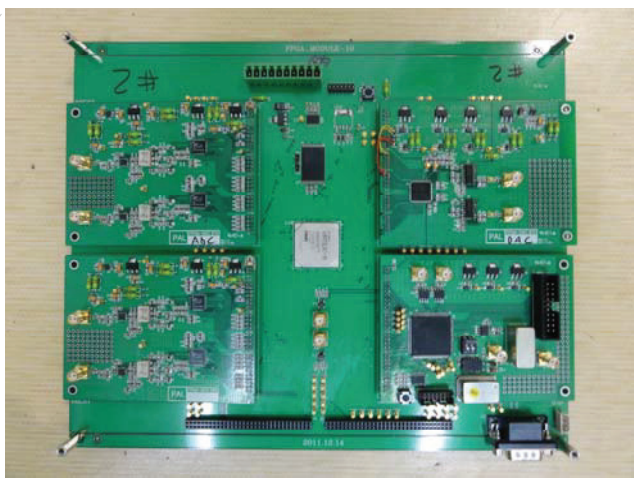

Figure 3 : Printed circuits board for the LLRF system: Left two daughter boards are the ADC, right upper board is DAC, right bottom is the clock generator and digital input and output and two connectors at bottom are spare for the other functions.

The LLRF system was designed to support both direct digital synthesizer(DDS) and an analog IQ modulator using the AD8345 from Analog Device Co.

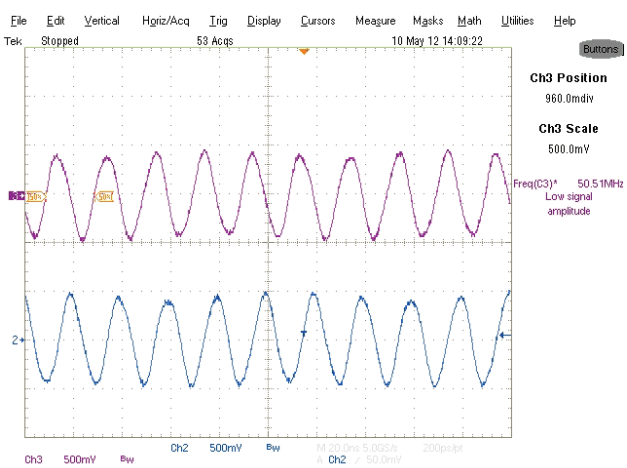

Figure 4 : DDS output signals of the sine and cosine function corresponding to I and Q.

The 50MHz of IF using the DDS method is generated as $F_{IF} = M \times F_{DAC} / 2^N$, where M is 5, N is 4 and F_{DAC} is 160MHz. Then the phase increment at this condition is given to 112.5°. Figure 4 shows the DDS output of the sine and cosine signal generated by the FPGA board. The DAC of AD9747 from Analog Device has dual channels inside with 16-bit resolution and 250Msps. The one of dual channels is assigned to generate the control signal and the other is for the signal monitor or diagnosis when DDS mode selected. If the analog IQ modulator was decided to the LLRF system, then two channels will charge I and Q output signal, respectively.

Clock generator

There are some clocks to need for LLRF system for ADC & DAC clocks and an IF to generate a LO. A Spartan6 FPGA was adapted for the clock generation, which has PLL and Digital Clock Managers (DCM) in its function. The reference clock came from either an internal XCO of 10MHz or an external source. The clock generator has two stages. The first is PLL stage, which includes several stage such as phase-frequency detector, charge pump, low pass filter and voltage controlled oscillator. The second stage is the DCM, which output frequency is defined as $F\_out = F\_in \times M/D$ where M = {2..256}, D = {1..256} and F_in is the output of the PLL. With cascaded two stages of PLL and DCM, Spartan6 can generate any frequencies that needed in the LLRF. Figure 5 shows DAC clock, ADC clock and IF generated by the Spartan6.

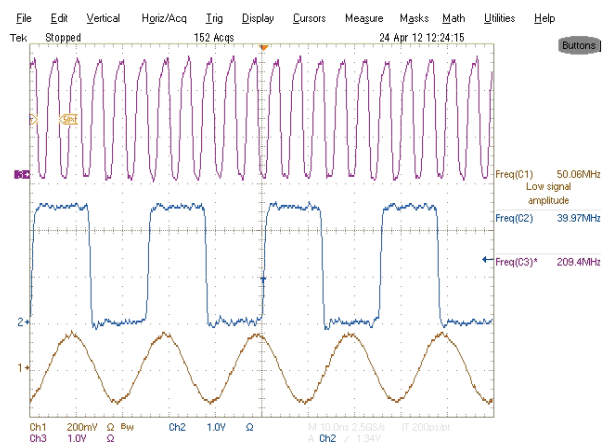

Figure 5: Signals generated by the Spartan6 for DAC, ADC and IF.

Microblaze Processor

The new trend of the FPGA application is to embed the flexible CPU into the FPGA device. The Microblaze soft process was accepted for the LLRF system at many accelerator laboratories. The configuration of the Microblaze can easily be changed by the selecting the IO functions provided by the Xilinx Co [3]. The Microbalze processor provided by the Xilinx was adopted for the

interface between the LLRF logic and the consol computer. The Microblaze receives serial data from the remote console and transforms it to the 32-bit data frame for the FPGA so it makes the VHDL program simple and gives flexibility to the interface program because it uses C language. Data exchange between Micorblase and VHDL uses the flags for both directions.

The timer interrupt was also configured to get the data from the FPGA logic and scan the digital input status, periodically. The slow interlock signals may be connected to the Microblaze processor.

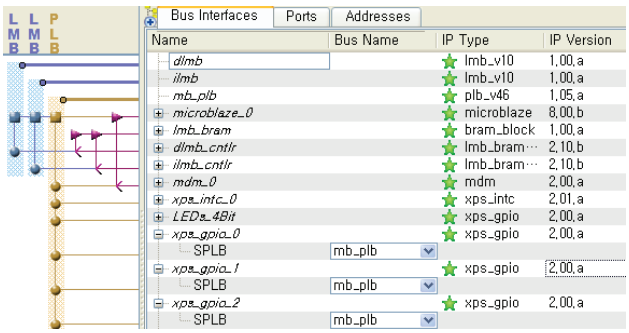

Figure 6 : Bus connection of the Microblaze for the LLRF.

Filters Simulation

There are three kinds of filter that used to be implemented in the LLRF application like FIR, IIR and CIC. An average method sometimes applied to the LLRF signal processing. Each one has merit and demerit comparing to the others. The output response of the IIR has distortion at the passband region while the filter order is relatively small. The FIR has a flat and linear phase response at the passband but filter orders are about ten in order to get the useful output responses. So it takes a longer time for calculation. The CIC has no multiplication in its calculation, but it also has non-linearity in its passband region. All the mentioned filters were simulated to confirm its frequency responses using the MATLAB. After those works, they were written in VHDL code and also simulated with ISIM. Figure 7 shows the simulation process of the FIR filter which is coded for LLRF.

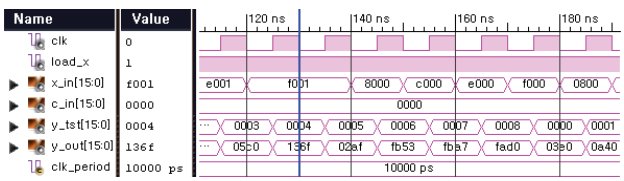

Figure 7 : FIR filter simulation using the ISIM.

CORDIC calculation

The Cordic algorithm provides to calculate trigonometric functions, such as cosine and sine, by using only shift and add operations. It takes a short time in calculation for the digital signal processing, thus it has been adapted in the LLRF system.

The vector R can be made to rotate through any arbitrary angle by a series of rotations according to

$$\theta = \sum_{i=0}^{N} \theta_i \,,\ 0 \le \theta \le 90^o \ \text{ where } \ \Delta\theta_i = \tan^{-1}(1/2^i)$$

The Cordic algorithm is given as the following equations

$$x_{i+1} = x_i - \delta_i y_i 2^{-i} \,,\ y_{i+1} = y_i + \delta_i x_i 2^{-i}$$

Where $(x_0, y_0) = (K, 0)$, $z_0 = \theta$, $K = 1/\prod_{i=1}^{N} \sqrt{1+2^{-2i}}$,

and $z_{i+1} = z_i - \delta_i \arctan(1/2^i)$. There are two modes in the Cordic algorithm. The rotation mode is given when $\delta_i = \text{sgn}(z_i)$, and vectoring mode is $\delta_i = -\text{sgn}(y_i)$. The table 2 shows the differences between reference values and simulated outputs when the Cordic order is 12 in the rotation mode. The maximum error shows 0.0895%.

Table 2: Error of the Cordic simulation with the reference.

Input θi	Reference		Output		Error(%)	
	cosθ (X axis)	sinθ (Y axis)	cosθ (X axis)	sinθ (Y axis)	cosθ (X axis)	sinθ (Y axis)
45	0.70711	0.70711	0.70709	0.70715	0.0014	0.0047
10	0.98481	0.17365	0.98474	0.17365	0.0067	0.0003
20	0.93969	0.34202	0.93945	0.34222	0.0239	0.0204
30	0.86603	0.50000	0.86603	0.50006	0.0002	0.0061
40	0.76604	0.64279	0.76599	0.64288	0.0053	0.0096
50	0.64279	0.76604	0.64288	0.76599	0.0096	0.0053
60	0.50000	0.86603	0.50006	0.86603	0.0061	0.0002
70	0.34202	0.93969	0.34113	0.94006	0.0895	0.0371
80	0.17365	0.98481	0.17365	0.98474	0.0003	0.0067
90	0.00000	1.00000	0.00000	0.99994	0.0000	0.0061

CONCLUSION

A digital controlled LLRF system based on a FPGA has been developing for PLS-II superconducting RF cavity. The LLRF system includes Vertex6 FPGA for control and arithmetic calculation. Four ADCs with 16-bit resolution are implemented for IQ demodulation. The DDS for vector output by the high throughput DAC was assembled and tested. The local clock generator for system clocks like, DAC, ADC and IF was designed and tested using the Spatan6 FPGA. A Microblaze processor was accepted for interfacing between console and FPGA logics, thus it gives the LLRF system more simple and flexibility in VHDL programming. Almost all functions for building the LLRF system such as FIR, IIR, CIC, Vector sum, PI, CORDIC and so on are coded using the VHDL and simulated by the ISIM, Simulink and Matlab.

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