LLRF CONTROL ALGORITHM FOR APEX *

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Abstract

The Advanced Photo-cathode EXperiment (APEX) is an ongoing experiment of a high repetition rate low emittance VHF band gun [1]. A low level RF (LLRF) control and monitoring subsystem is developed based on 5 LLRF4 [2] boards. One of them is used for low level RF control and the other 4 are used as interlocks and RF monitors at different points of the system. The synchronization of the photocathode laser is also controlled relative to the RF system. This paper summarizes the control algorithms implemented in the system firmware.

INTRODUCTION

APEX uses a VHF gun to generate high repetition rate low emittance electron bunches. The first stage of the experiment is conditioning the cavity under high power, and then testing the cavity together with the drive laser to generate the desired electron pulses.

The cavity nominal resonance frequency is 186 MHz, and the laser repetition rate corresponds to the fifth subharmonic of the RF frequency (37.2 MHz). We detect laser photo diode signal at its fifth harmonic frequency which is equal to the RF frequency. A picture of the cavity installed in the BTF is shown in Figure 1.

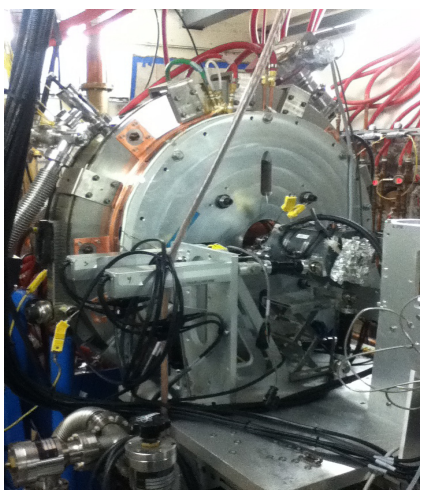

Figure 1: APEX cavity installed in BTF.

The basic requirements for the LLRF system are to provide an adequate RF drive signal to the high power amplifier, monitor the system status and provide fast interlocks, maintain synchronization between the drive laser and RF cavity, and provide a user interface to monitor and control the system. Currently, the cavity frequency tuner has not been installed yet, so the RF drive frequency must be adjusted to follow changes in the cavity resonance frequency.

The LLRF system for APEX consists of one RF control chassis and two monitor and interlock chassis. The RF control chassis drives a solid state amplifier followed by a 60 kW tetrodes to feed the cavity, and it also phase locks the laser to the same cavity frequency. The monitor and interlock chassis monitor multiple points along the RF distribution line and provide interlock signals. The cavity is fed by two symmetric input couplers, so the RF drive signal is split and amplified separately.

In each of these chassis, the RF signal are mixed with a common Local Oscillator (LO) to generate the Intermediate Frequency (IF) signal, one (for the RF control) or two (for the interlock and monitoring) LLRF4 boards are used to process the IF signal and generate control signal accordingly. The FPGA (Xilinx XC3S1000) and ADC clock is $f_{\rm clk} = 100\,{\rm MHz}$. The ADC digitize the IF frequency and feed the data to the FPGA to be processed. The LO frequency in the chassis is twice the clock frequency. The nominal relationship between the RF/laser frequency and the clock frequency is

$$f_{\rm IF} = f_{\rm clk}/7 = 2 \cdot f_{\rm clk} - f_{\rm RF} = 14.3\,{\rm MHz}$$

Each LLRF4 board has 4 IF input channels, so altogether there are 20:

LLRF control chassis cavity cell 1, laser, cavity forward 1 and cavity reflect 1

monitor and interlock chassis 1 board 1 cavity cell 2, cavity forward 2 and cavity reflect 2 and one spare channel

monitor and interlock chassis 1 board 2 circular forward and reflect for 1 and 2

monitor and interlock chassis 2 board 1 solid state amplifier forward and reflect for 1 and 2

monitor and interlock chassis 2 board 2 tetrode amplifier forward and reflect for 1 and 2

All of the 5 LLRF4 boards interface with a Linux computer through USB ports. On the host computer, an EPICS IOC driver is designed to provide access to the FPGA registers through EPICS process variables (PVs). The same firmware runs on all LLRF4 boards; each board has its own USB ID and its own initial register settings.

APEX DSP BLOCK DIAGRAM

The APEX LLRF DSP block diagram is shown in Figure 2. There are three generic signals routed to many modules.

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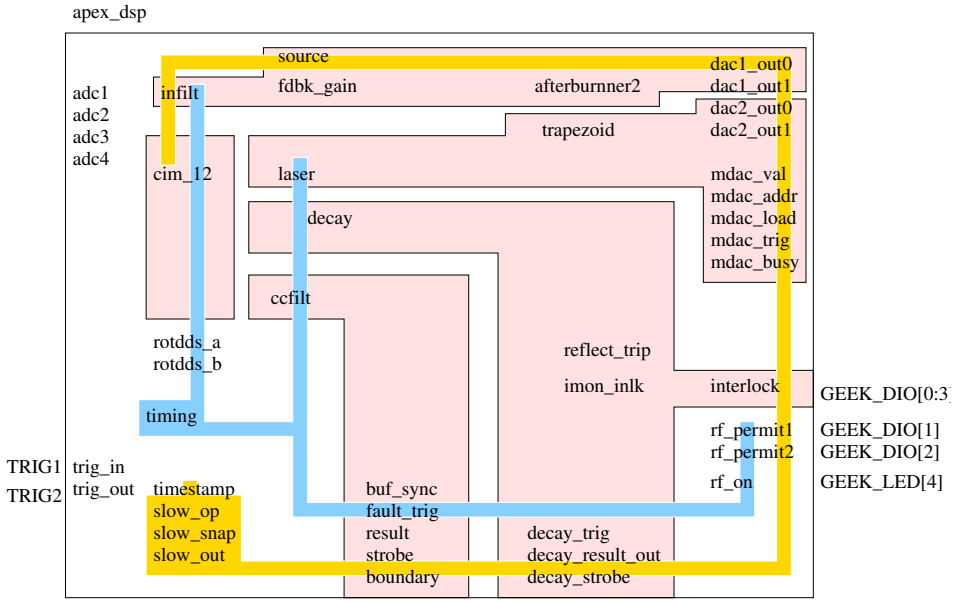

Figure 2: APEX DSP block diagram.

The timing strobe for each module is generated and fed each module. Slow monitoring points are attached to an 8-bit wide shift register for easy routing and connection to the final data stream. The control from host via USB is converted to a write-only local bus with 32 data bits and 7 address bits.

Two Direct digital synthesizers (rotdds) are used in the code as the digital LO for the digital down converters. One of them is set at RF frequency as the LO. The 4 digitized IF inputs and the IF drive output are connected to the digital mixer, and mixed with the common LO to get an in phase (I) component and quadrature (Q) component. The other DDS is intended for electronics characterization; it has a dedicated LO which can be tuned to detect harmonics and interference lines. The RF input of that mixer is software-selectable among all of the IF inputs. The 12 integral results are serialized before being decimated and comb filtered. The fast waveforms are fed to buffers implemented by dual port RAMs: a large circular buffer for general use, and a separate buffer dedicated for the cavity decay waveform.

The APEX LLRF DSP implements following features as shown in Figure 3.

1. waveform monitor and fault record
2. waveform analysis and interlock signal generation
3. synchronize the laser to the RF
4. RF amplitude and phase control

Features 1 to 3 require further mix of the IF signal and low pass filtering down to baseband. They can share a common mixer and integral module, the decimation ratio will be different but share a common factor of 14. Assuming the IF input is $V_{\mathrm{IF}} = A\cos(\omega_{\mathrm{IF}}t + \phi)$, mix it with the digital LO signal derived from the FPGA clock $V_{LO} = Bcos(\omega_{IF}t)$, we get

$$\frac{AB}{2}\cos(2\cdot\omega_{\mathrm{IF}}t + \phi) + \frac{AB}{2}\cos(\phi)$$

The mixer result is low pass filtered by a two stage CIC filter, which also filters out harmonic frequencies. The CIC filter transfer function is

$$\frac{(1-z^{-R})^N}{(1-z^{-1})^N} = \left(\sum_{k=0}^{R-1} z^{-k}\right)^N$$

where R is the sampling rate change, in our case they all share the common factor of 14. The integrator output have a gain of $(R)^2$. We limit the R to $64{*}14$, which already provide enough zoom range for operator to zoom in and out. After the comb part of the filter, we need to shift according to the R value to maintain resolution and avoid overflow.

For the waveform monitor, the decimation ratio can be set by the user using the GUI, then the output of the comb needs to be shifted accordingly to avoid overflow and maintain enough accuracy. An extra half-band filter is used after the CIC filter to give sharper suppression of aliased frequency components. All 6 I and Q pairs are processed and transfered out as waveforms.

For cavity decay waveform analysis, the decimation ratio is fixed, since the cavity decay time constant is known (approximately) *a priori*. The decay waveforms are transferred to the host computer to analyze the cavity characteristic frequency (relative to the LO). In the future, this information will be used to calculate the cavity tuner drive signal. For now, the system adjusts the DDS frequency to follow the cavity frequency drift. The reflection waveform amplitude is compared with a threshold; if reflection is higher than expected, taking into account the filling transient, then the reflection fault is triggered. For the monitor

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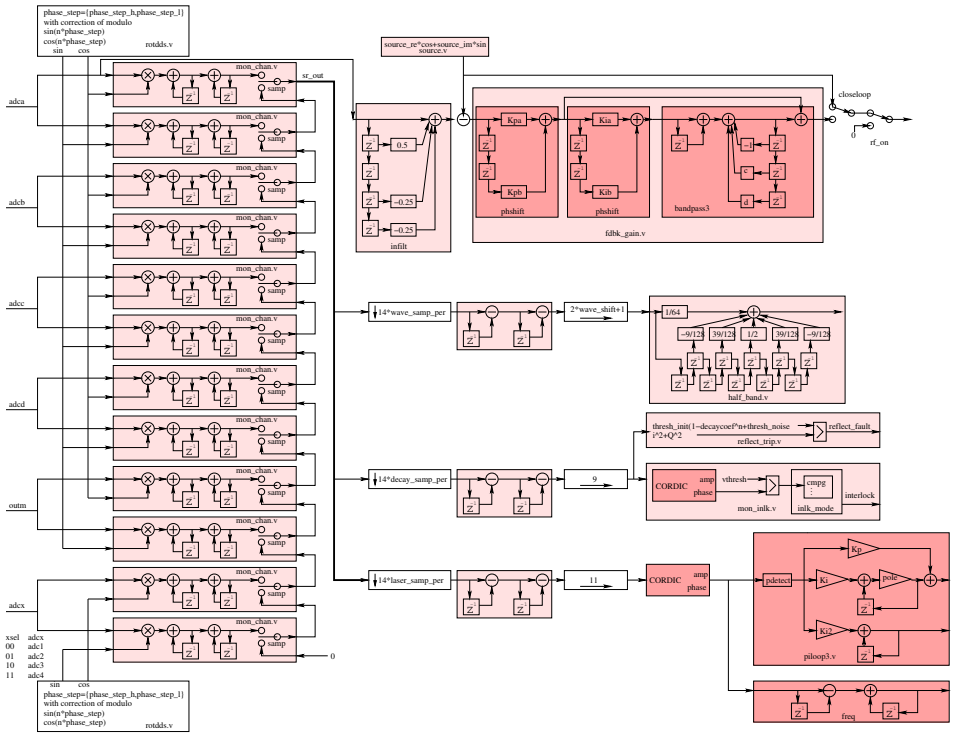

Figure 3: APEX DSP implementation.

and interlock chassis, all the input waveform amplitudes are calculated by a CORDIC [3] and compared with an upper limit and a lower limit for each signal. Then the user can select when to trigger an interlock trip, the options are higher then upper, lower then lower, within or outside of the range between upper and lower.

For the laser synchronization, the decimation ratio is also fixed and set to be low to achieve high control bandwidth. Amplitude and phase are measured by a CORDIC and the received phase is used as the error signal for a Proportional-Integral (PI) controller. The calculated control signal is used to drive the laser fast piezo. An extra integral loop is used to calculate the drive signal for the laser slow piezo.

The RF pulse width and repetition rate can be set from the user GUI. The amplitude and phase control is implemented directly from the non-IQ ADC readings [4], without downconversion and CIC filtering, to keep latency small. The overall feedback system transfer function is

$$\left(K_{p,\alpha} + K_{p,\beta}\, z^{-2}\right)$$
$$\left(1 + \left(K_{i,\alpha} + K_{i,\beta}\, z^{-2}\right) \frac{1 - z^{-1}}{1 - z^{-1} + c\, z^{-2} + d\, z^{-3}}\right)$$

GUI SUPPORT

At the host computer side, each board runs an IOC driver. An engineering GUI is provided together with the software firmware development platform to access registers of that board. A user GUI is written in MATLAB to combine information from all 5 IOCs, including display of all 19 RF channels different tabs. An example of the user GUI is shown in Figure 4.

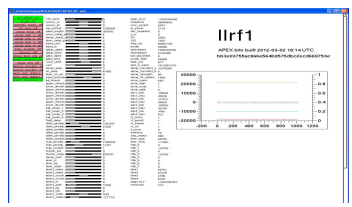

Figure 4: APEX LLRF control user GUI.

SUMMARY

The APEX LLRF control system has been used during cavity high power conditioning. The photocathode laser has been synchronized with the RF. Tests of the RF vector feedback need to be arranged.

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