A COMPACT SWITCHING POWER SUPPLY UTILIZING SIC-JFET FOR THE DIGITAL ACCELERATOR *

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Abstract

Utilizing a high power discrete SiC-JFET developed by KEK, a switching power supply (SPS) that had a circuit topology of H-bridge was designed and constructed to drive the induction acceleration system for the KEK digital accelerator. The SPS was operated with a 38 Ω dummy resistance load and bipolar outputs of 800V and 21A were successfully demonstrated at 1 MHz.

INTRODUCTION

The KEK digital accelerator (DA) shown in Fig.1 is a small-scale induction synchrotron (IS) without a high-energy injector [1], where an induction cell is employed as an acceleration device. The concept of an IS was experimentally demonstrated in 2006 [2] through the use of the KEK 12 GeV PS. Commissioning of the DA is going on now [3]. The DA has no limitation of bandwidth in a lower side because the induction cell is a simple transformer driven by a switching power supply (SPS) that generates bipolar pulses. The present SPS, which is composed of 7 series connected MOSFET per one arm of a H-bridge because of the limitation of a heat deposit capacity and a withstand voltage of the MOSFET , carries an arm current of 20 A at 2 kV. Series connection of the MOSFETs has substantially induced a large complexity in handling gate trigger pulses.

To solve these problems, the next generation of switching pulse modulator utilizing silicon carbide (SiC) devices is under development. The SiC device seems to be a promising candidate because advanced electrical and material properties of SiC power devices [4] allow us to realize a more reliable SPS with desired essential features. The SiC power semiconductors are characterized by outstanding performance in their high voltage blocking capability, low voltage drop in their on-state, less switching time and thermal resistance. The conduction and switching losses can be notably reduced and the limitation of operating temperature can be significantly mitigated, compared to Si devices. These robust and low loss characteristics of SiC devices are desired for the application in the digital accelerator. Unfortunately, a SiC-JFET suitable for high power applications has been commercially unavailable. In such a situation, the authors initiated the development of a new device package suitable for the application of ISs and demonstrated a good yield rate and achieved successful test results of 1 MHz-1 kV-27 A operation [5].

Following the successful results of the device evaluation, they designed and constructed a SPS that had a circuit topology of H-bridge. In this paper, design and test results of the SPS are described.

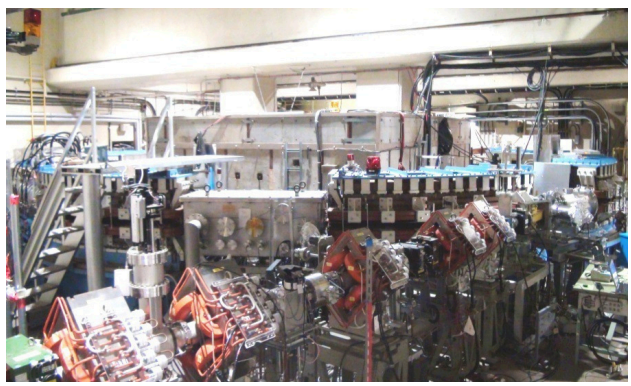

Figure 1: Photograph of the KEK-DA.

Figure 2: Photograph of the existing switching power supply (SPS) employing MOSFETs.

DESIGN OF THE SPS

SiC-JFET

Figure 3 shows the package of the SiC-JFET (completed and before molded). The device is assembled on a 58 mm x 36 mm copper base plate and has the height of 7 mm. The device performance is summarized in Table 1.

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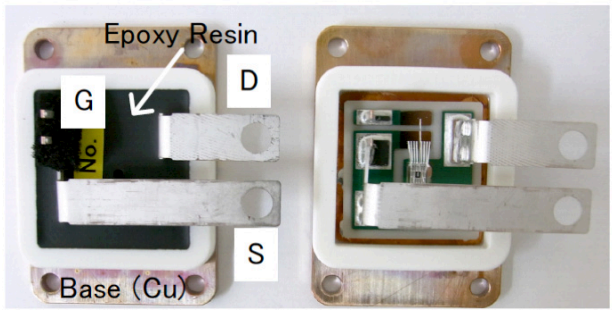

Figure 3: The developed SiC-JFET package.

Table 1: Device Performances

Parameter	Value	Unit
Blocking voltage	1200	V
Pinch-off voltage	-17	V
On resistance (@150℃)	0.2	Ω
Thermal resistance, junction to case	0.56	K/W
Power dissipation	>250	W

SPS

The SPS has a configuration of H-bridge. Figure 4 shows a schematic diagram of the SPS. The H-bridge has 4 switching arms , each of which is composed of a SiC-JFET that is mounted on a water-cooled heat sink and a gate drive circuit connected to an insulated dc power supply and is triggered by a light signal. Also each arm has a snubber circuit, which has a role of absorbing a discharge energy stored in the parasitic circuit inductances and is composed of a capacitor Cs, a diode Ds, and a Resistance Rs.

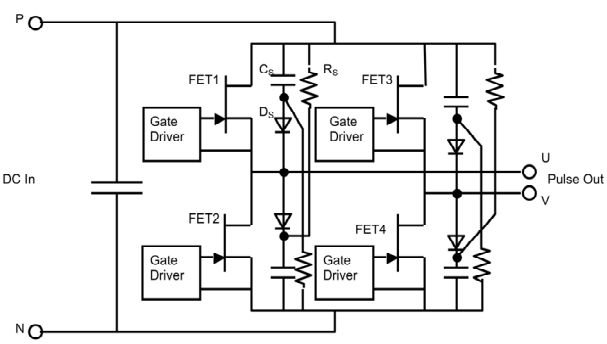

Figure 4: Schematic diagram of the SPS.

In high speed switching application, decreasing a stray inductance is quite important to diminish an unexpected voltage oscillation or over-voltage. To diminish such a parasitic inductance, a lapped capper plate interleaving with two Nomex® papers, which has a thickness of 0.25 mm, were used. Figure 5 shows a planar layout of the capper plates and dominant circuit components.

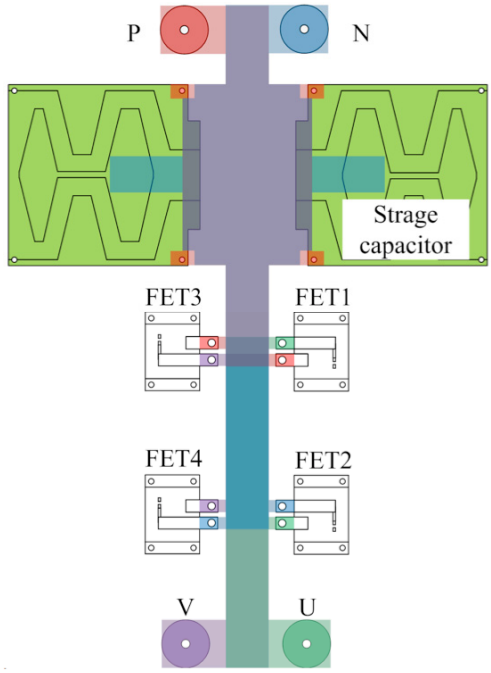

Figure 5: A planar plan of the SPS.

TEST RESULTS

Switching Waveform

Figure 6 shows a output current pulse and a voltage waveform between Drain and Source of FET1 under the condition of DC input of 800 V and the repetition frequency of 1 MHz. Some oscillation was observed in the voltage waveform, and thereby the peak voltage V_{dsp} exceeded the dc input voltage. This oscillation is caused by discharged energies stored in the parasitic inductance and capacitance of the circuit. To analyze this phenomenon, a circuit simulation was carried out using the circuit model shown in Fig. 7, where circuit parameters were semi-empirically determined. Simulation results are shown in Fig. 8, where voltage-oscillation similar to that of the measured waveform was obtained.

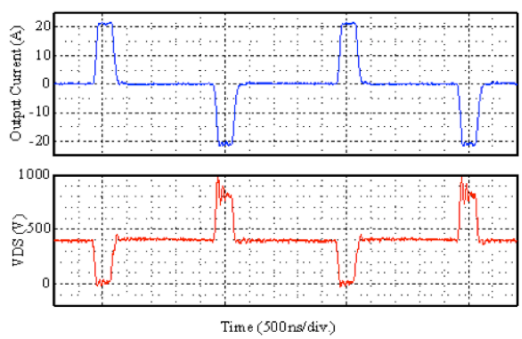

Figure 6: Measured waveforms. Upper trace: output current pulse. Lower trace: Voltage waveform of FET1.

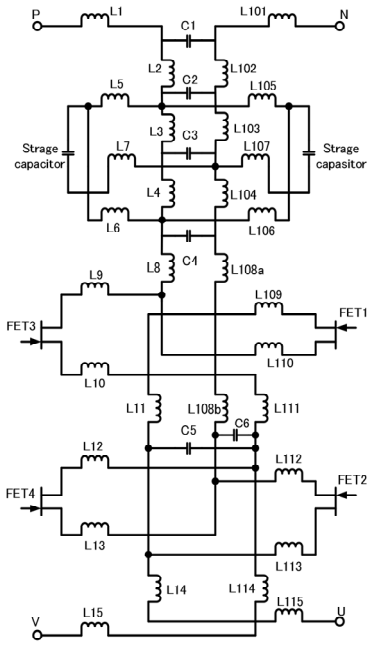

Figure 7: Circuit simulation model.

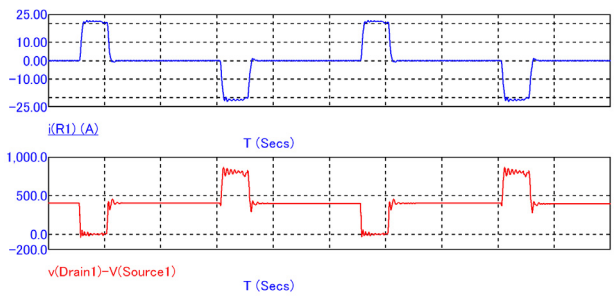

Figure 8: Simulated waveforms. (200ns/div.). Upper trace: output current pulse. Lower trace: Voltage waveform of FET1.

Vdsp of FET1, FET2, FET3, and FET4 were compared between the measured value and simulated value. The results are shown in Table 2. Measured values are higher than simulated values generally. Moreover, Vdsp of FET1 and FET2 was higher than that of FET3 and FET4 in both measured and simulated.

Table 2: Measured Value and Simulated Value of Vdsp

FET	Measured Value (V)	Simulated Value (V)
FET1	966	862
FET2	955	873
FET3	895	831
FET4	894	851

Temperature Rise

Figure 9 shows temperature rise curves of the FET1 during 1 MHz continuous mode operation with various dc voltages. The temperature was measured at the top surface just above the device die using a fluorescence type thermometer. Increasing rate of the temperature was steep in first 1 minute, and then decreased because of the temperature rise of cooling water. Finally, it arrived at a steady state after the temperature controller of cooling water began to start. Even in Vdc of 800 V case, the maximum temperature rise was under 35 K, which was rather lower than that of the device's limitation. Thus we concluded that the temperature margin was sufficient.

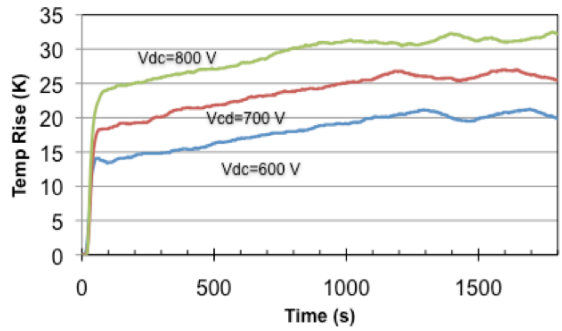

Figure 9: Temperature rise of the JFET. Upper : output current pulse. Lower): Voltage waveform of FET1

SUMMARY

- Utilizing a high power discrete SiC-JFET developed by KEK, a switching power supply (SPS) that had a circuit topology of H-bridge was designed and constructed.
- The SPS was tested with a 38 Ω dummy resistance load and successfully operated at 1MHz-800V-21A bipolar outputs.
- Measured and simulated waveforms exhibited a fairly good agreement.
- During a 1MHz continuous mode operation, temperature rise of the switching device was sufficiently low.

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