# SEQUENCER DESIGN OF TIMING SYSTEM FOR THE TAIWAN PHOTON SOURCE

C. Y. Wu, Jenny Chen, Y. T. Chang, Y. S. Cheng, P. C. Chiu, C. Y. Liao, K. H. Hu, C. H. Kuo, K. T. Hsu
NSRRC, Hsinchu 30076, Taiwan

*Abstract*

The timing system of the Taiwan Photon Source (TPS) is used to distribute trigger signals and synchronously clocks to all the equipment of the machine which need them. The timing system basically works by sending event codes from one event generator (EVG) through tree structured, bidirectional optical fiber network to many event receivers. To accommodate various operation and injection scenarios of the TPS storage ring, booster synchrotron and linear accelerator, timing sequencer design and control is crucial. The sequence (event code) is stored at sequence random access memory (RAM) of the EVG module. In order to manage sequence RAM of EVG, the timing sequencer control is considered to use EPICS sequencer running in the timing master EPICS IOC. The sequencer design of timing system will be summarized in this paper.

## INTRODUCTION

The TPS is the latest generation synchrotron light source under construction and commissioning, and is planned in 2014. Event based timing system will apply for TPS [1-3]. The implementation of timing system is in proceeding. The test system already applied for the TPS 150 MeV linear accelerator (linac) commissioning and acceptance during the second quarter of 2011. Various support for the timing system are in preparation. The timing system is based on the events coming from event generator. EVG handles the accelerator synchronization and trigger the injection and the extraction pulse device. In order to provide an efficient management of the sequence RAM in the event generator, the sequencer design of timing system is on going.

## TPS EVENT SYSTEM

The TPS timing system is an event based system. A central EVG generates events from an internal sequence RAM and external sources [4]. These events are distributed over optic fiber links to multiple event receivers (EVRs) [5]. The EVRs, which are located in the control system interface layer, decode the events referred to as hardware triggers or software interrupts. For the linac, the decoded events are further encoded by a gun transmitter and sent over a fiber link to the gun high voltage deck. The external event sources include pulse per second (PPS) signal which is locked to global positional system (GPS), AC mains 60 Hz trigger, post-mortem trigger after beam loss and machine protection system trip. The event clock is derived from the 499.654 MHz master oscillator so that it is locked to change in the RF frequency. The master oscillator can be used as an external reference from a GPS disciplined Rubidium 10 MHz clock. TPS timing modules include 6U CompactPCI form factor modules include cPCI-EVG-300, cPCI-EVR-300, cPCI-EVRTG-300 and linac gun trigger receiver. Add PCIe-EVR-300 to accompany with fan less embedded EPICS IOC for some applications is in plan. Configuration tools were developed. Save and restore supports are also available. Sequencer design is current work. Installation of the system is scheduled in mid-2013.

## DESIGN PHILOSOPHY OF THE TIMING SEQUENCER

Sequence RAM control of the injection scenario has been tested by Matlab script running in control console over Ethernet to change the sequence RAM of EVG in the timing master EPICS IOC. A prototype of sequence control by Matlab was tested [3]. The result is acceptable from the performance point of view. However, to provide more flexibility environment, the EPICS sequencer seems more efficient work at the IOC level. The timing sequence control is based on state machine. The timing sequencer will defined several PVs for define the transition among different states to communicate with another IOCs. The sequence RAM will disable by the stop interrupt of the sequence RAM and replace sequence RAM contents.

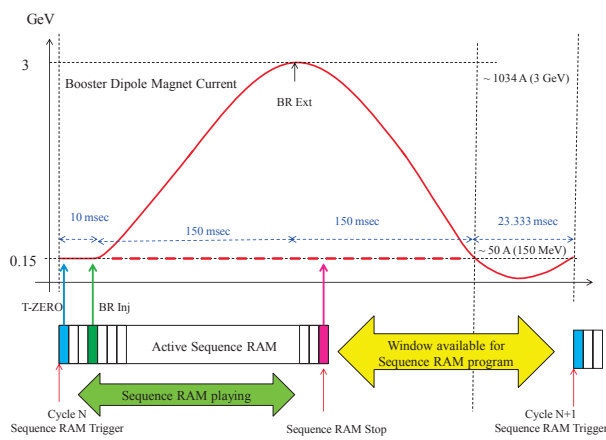


Figure 1: Typical booster synchrotron modified sinusoidal ramping scheme.

The TPS accelerators will be operated in 3 Hz repetition rate. The booster power supply ramping waveform could be sinusoidal wave or quasi-sinusoidal with injection flat. The quasi-sinusoidal with injection flat provides flexibility for the booster tuning and can be done




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in DC mode, ramping can be performed just active ramp trigger as shown in Fig. 1.

The sequence is started at T-ZERO which is the trigger time of the sequence RAM and start time of a new accelerator cycle. Energy ramping time of the booster synchrotron is about 150 msec when repetition rate set at 3 Hz. The sequence RAM will stop after the booster synchrotron finish the ramping cycle. There are more than 100 msec time window available for change contents of the sequence RAM. Using EPICS sequencer to program sequence RAM after the sequence RAM stop. The timing sequencer will be running in the timing master EPICS IOC for sequence RAM controlling to satisfy the machine operation. All parameters for the machine operation modes will be designed as specific EPICS PVs, such as operation modes, e-gun modes (single bunch or multi-bunch), bucket address, repeat cycle, top-up injection, decay mode and etc. Timing sequencer structure is presented in Fig. 2.

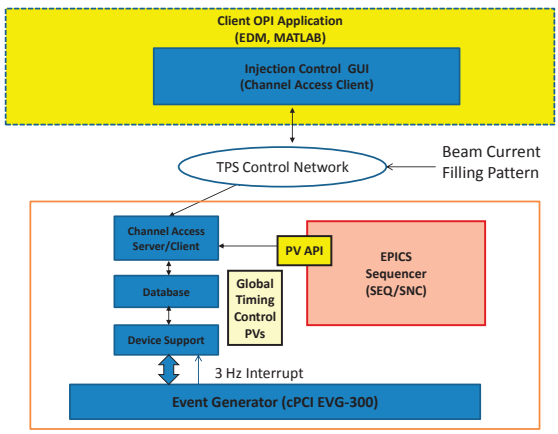


Figure 2: Timing sequencer structure.

### *Sequence RAM Trigger*

The sequence RAM will trigger by the 3 Hz rate which are generated by synchronize with the sync of booster, storage ring revolution frequency and the 60 Hz mains frequency. Trigger at another repetition rate can be changed if it is necessary. The booster synchrotron will work at 3 Hz rate normally.

### *Sequence RAM Entry and Timestamp Management*

All sequence will store at the sequence RAM. There is a timestamp associated each entry. The event can be active when load the desired timestamp. The event can be de-active by replacing the event code as NULL event (event code: 0x00), it can active again when the NULL event is replaced by original event. The timestamp value can be changed for budget address requirements. The sequence RAM will program in every cycle. All kind of the operation can be fulfil by these mechanism. The clients can control the timing sequencer to change contents in every cycle via pre-defined PVs. The example of sequence RAM management is presented in Fig. 3.

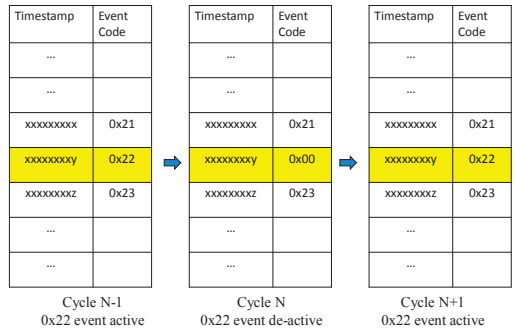


Figure 3: Sequence RAM management: individual trigger event control.

### *Sequence RAM Programming*

The sequence RAM contents can be updated when current cycle stop. The programming can be done within a few msec. It can program cycle-by-cycle at 3 Hz rate easily.

## INJECTION CONTROL

Injection control is the main theme of the timing system. Timing events related to the operation of all devices will be defined and associated to a timestamp to specify its happened time. To satisfy individual operation of subsystems, coordinate injection process, various trigger events might need enable and/or disable. To provide bucket addressing, the timestamp of some trigger events need to adjust cycle-by-cycle dynamically. The timing sequence will be stored at the sequence RAM in the EVG. The sequence will play every accelerator cycle trigger happed in 3 Hz rate. The timing sequencer will re-program sequence RAM according to next cycle requirement after current cycle sequence RAM stop.

There are several IOCs involved the injection process including timing master IOC, booster main power supply IOC, booster RF IOC, NPCT IOC, filling pattern IOC, injection and extraction pulse magnets timing IOC. Relationship of injection control related IOCs is shown in Fig. 4. The linear accelerator and e-gun trigger are located at the timing master which will install at the equipments area (Control Instrument Area, CIA in TPS location name convention) just at roof of linear accelerator system.

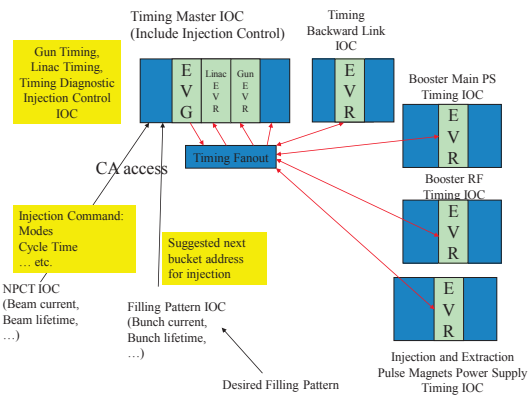


Figure 4: Relationship of injection control related IOCs.

### *Operation Mode*

Software configurable sequence RAM provides a flexibility to change the operation modes. It just needs resource to development. Basic operation will support at commissioning phase. Sophisticated modes will delivery later. A simple configuration tool should be available for sequence RAM management. The possible operation modes include:

- Accelerator hardware test mode.
- Individual subsystem trigger.
- Single shot.
- Continue injection.
- Repetitive rate decimation for specific trigger.
- Warm up trigger for specific device.
- Top-up for desired fill pattern.
- Top-up with filling pattern feedback.

### *Bucket Addressing*

The bucket addressing will be preformed to change the value of timestamp via timing sequencer at every cycle. Change one count corresponding to 8 nsec which is the period of the event clock ($f_{RF}/4$) used by the TPS event system. Bucket addressing scheme is shown in Fig. 5. Fine delay needs change the correspondent of the gun trigger delay in cPCI-EVRTG-300 and digital delay generator for the storage ring injection kicker trigger.

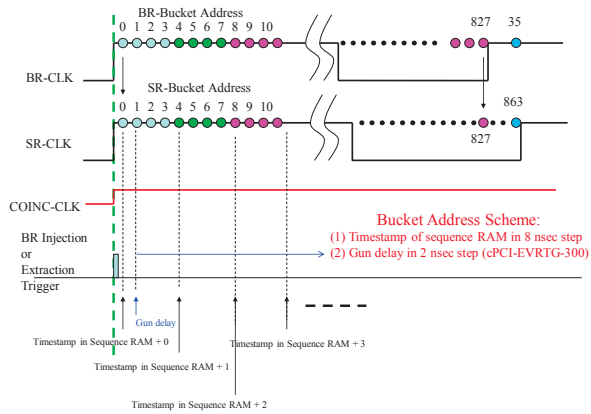


Figure 5: Bucket addressing scheme for TPS.

### *Top-up Injection with Bucket Addressing*

The top-up injection scheme might adopt multi-bunch mode to injection beam to desired target current and switch into the single bunch mode. The averaged and bunch current monitor will be calculated the bunch current and suggest the bunch with minimum bunch current for next injection.

### *Beam Repetition Rate Control*

To reduce unnecessary radiation dosage produce, the beam repetition rate can be decimated by disable some e-gun trigger of accelerator cycles upon request. This can be achieved on the configure page.

### *Filling Pattern feedback*

In order to minimize fill pattern correlated orbit oscillations due to uneven bunch patterns, filling pattern control and/or feedback is planned to minimize bunch-to-bunch variation of bunch current. Therefore the filling pattern IOC will measure bunch structure of storage ring and suggest next injection bucket address to timing master IOC via PV channel access.

### *Miscellaneous Considerations*

Some devices might need trigger a few cycles for warm before it reaches stable working conditions for beam injection. For example, injection septum of the storage ring might need to trigger one or more cycles before it reach to the stable conditions. This is happened in several light sources. The timing sequencer can program the septum fire one or more cycles before real injection cycle take place. The booster power supply might need to run one or several cycles before it reaches a condition suitable for beam injection. This mechanism can ensure accelerator working properly before beam inject.

### *Implementation*

The timing sequencer will code by state notation language (SNL) with the EPICS sequencer. Communication with client application via defined PVs, these PVs include e-gun trigger mode, multi bunch length, operation mode, bucket address of next cycle … etc.

## CURRENT STATUS

The implementation of the timing system and timing sequencer is ongoing. Various operation scenarios are analysis thoroughly. Prototype test by Matlab scripts was tested in 2011. Change to EPICS sequencer by program using SNL is on-going.

## ACKNOWLEDGEMENT

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