STATUS OF THE MIXED-SIGNAL ACTIVE FEEDBACK DAMPER SYSTEM FOR CONTROLLING ELECTRON-PROTON INSTABILITIES FOR THE SPALLATION NEUTRON SOURCE*

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Abstract

As the beam intensity at the Spallation Neutron Source (SNS) in Oak Ridge National Laboratory (ORNL) is increased, it becomes necessary to have greater control over the electron-proton (e-p) instability. This paper presents the design of a mixed-signal transverse feedback system for active damping of the e-p instability. It describes the design, features and results of this feedback damper, and it reviews several experimental studies to understand the system performance and its limitations. The mixed-signal feedback damper system employs power amplifiers (PAs), analog-to-digital converters (ADCs), multiple field programmable gate array (FPGA) chips, and digital-to-analog converters (DACs) to provide feedback damping and system monitoring. Unlike existing analog damping systems, FPGA-based feedback damping systems offer programmability while maintaining high signal processing performance. The system gain, delay and digital signal processing components can be programmed during the experiment to perform timing adjustments, correct for ring harmonics, and equalize magnitude and phase dispersions.

INTRODUCTION

The Spallation Neutron Source (SNS) at the Oak Ridge National Laboratory (ORNL) is currently a 925 MeV accelerator with an accumulator ring used to provide 1 MW of beam to the target. The high beam intensity at SNS causes a rapidly-growing electron-proton instability. In this instability, low-energy electrons are captured by the potential of the passing proton bunch. These electrons are repelled by the space charge force towards the opposite pipe wall where they are lost, reflected, or produce secondary electron emissions. As the head of the proton beam comes around on the next turn, the process repeats. This repetition continues until the tail of the proton beam is driven to large amplitude and hits the vacuum chamber wall. The proton beam loss leads to a much larger production of electrons and a sudden catastrophic loss of the remaining beam.

Active feedback damping systems have been used effectively to mitigate narrow-band beam instabilities [1-2]. Most current beam feedback dampers are implemented using analog components, due to their low cost and less complex designs. Compared to analog systems, FPGA systems are less sensitive to noise and process variations. Their flexible reconfiguration features can be used to provide high throughput and low latency by implementing computationally intensive parts of the signal processing systems on dedicated FPGA resources. FPGA solutions provide higher performance for parallel computation than software solutions, and greater flexibility and programmability than ASIC solutions.

The basic functionality of the transverse beam feedback mechanisms involves detecting an error in the beam position at the pickup, processing this signal, and delaying it until the bunch arrives at the kicker for correction. The challenges associated with designing a transverse beam feedback damper are dealing with the large dynamic range of the pickup signal, maintaining the proper timing and phase advance from pickup to kicker, providing a large enough kick to the beam, and providing a means to diagnose the phase delay and gain as the accelerator parameters are tuned. A FPGA-based mixed-signal system is ideal for handling these challenges. This paper presents the mixed-signal damper hardware, the diagnostics software, and some of the beam transfer function experimental results that are used to analyze the feedback damper system.

MIXED-SIGNAL HARDWARE

The mixed-signal feedback damper configuration is shown in Figure 1. It consists of a pickup electrode, a 10-bit analog-to-digital converter (ADC), two FPGA chips, four banks of 512MByte DDR3 memory, two Ethernet modules, a 12-bit digital-to-analog converter (DAC), a kicker electrode, and a trigger card. All of the components except for the power amplifiers are VXI compatible. The FPGA board is connected to the computer by Ethernet cables. The FPGAs are controlled by LabVIEW software.

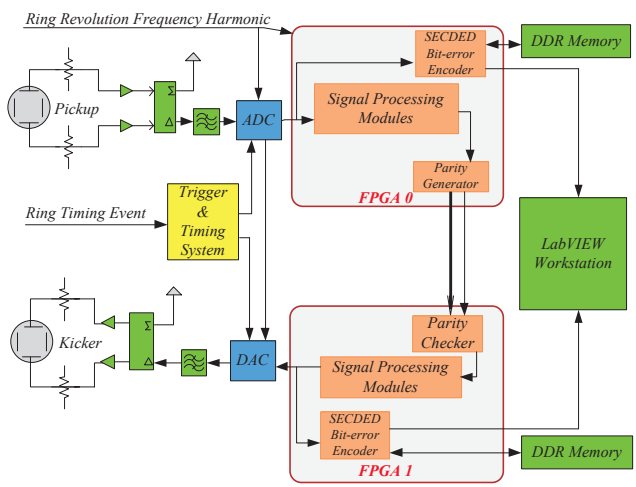

Figure 1: Schematic of the feedback damper system.

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Multiple FPGA System

Implementations of the feedback damper system on a single FPGA were explored in our previous work [3,4]. However, signal processing performance deteriorates rapidly when the available resources on the FPGA are used up. In order to increase the available FPGA resources and exploit parallel computation to handle the large dynamic range of the instability, the digital signal processing (DSP) modules are distributed on two FPGAs. The multi-FPGA design increases the overall delays in signal transmission and requires some FPGA resources to implement communication and synchronization logic in each FPGA chip. A schematic of the major blocks of the multi-FPGA design is shown in Figure 2.

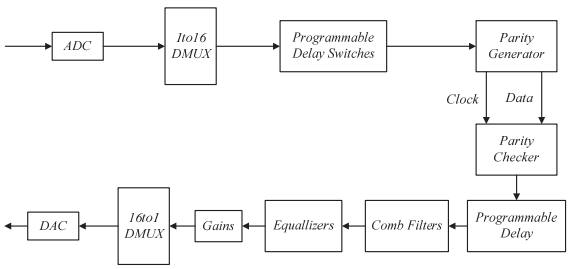

Figure 2: Schematic of the digital signal processing.

The purpose of the digital signal processing is to provide the proper gain and phase advance at all the betatron-coupled bunch frequencies to damp all of the modes. The digital delays are implemented as a programmable FIFO that maintains a phase difference of 90 degrees between the pickup and the kicker. The betatron tune at the SNS storage ring is considered to be a constant at each given beam energy. Therefore, proper measurement of the phase advance between the pickup and the kicker can be used to fine tune the digital delays.

To reduce the power that the system handles and to improve the cancellation of instabilities, comb filters are used such that poles are placed at the beam revolution frequency and its harmonics. To have stable filters with fixed feedback error, the comb filters are implemented in a feed-forward finite impulse response (FIR) form.

The equalizer is designed in an FIR filter form to compensate for the magnitude and phase dispersion. Designing an equalizer to cancel the phase dispersion improves the system performance by decreasing the power loss by about 10%. In [4], parallel FIR filters with different resource and performance tradeoffs are discussed in detail. The parallel FIR filters are the most computationally intensive module in the feedback damper system. Implementing a parallel 16-channel FIR filter with N taps requires a total of N·(27/16) multipliers. Therefore, it is necessary to limit the FPGA resources usage while maintaining signal processing performance. Figure 4 shows the magnitude and phase dispersion of our feedback damper system using equalizers when varying the number of taps. In our feedback damper system, a 32-tap, 16-channel FIR filter is adopted.

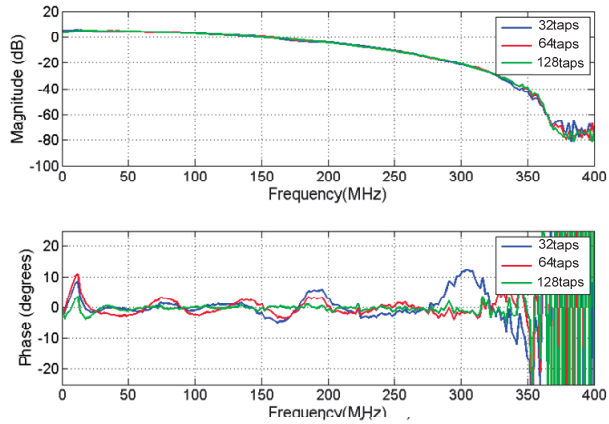

Figure 3: Feedback damper system magnitude and phase dispersion by varying the number of taps in the equalizer.

Trigger & Timing System

The ADC, DAC and the FPGAs are triggered by the accelerator event signals at 60Hz. The ADC and DAC are driven by a clock running at 1920 times the ring revolution frequency. Therefore, the digital clock source, controlled by a Digital Clock Manager (DCM), is synchronized to the ring frequency for the mixed-signal damper system to function correctly. The clock jitter, skew and any other problems related to clock synchronization are handled by the clock manager.

FEEDBACK MONITORING SOFTWARE

The FPGA-based feedback damper system uses a personal computer with a National Instrument NI-6601 digital I/O card and LabVIEW software for control. A series of software routines are developed in LabVIEW to adjust the digital gains, programmable delay (FIFO), comb filters, and equalizer coefficients. Given the information about the beam revolution frequency and the desired phase advance, the computer can set all the components' parameters for effective damping. Once the system has been configured for damping, it can run independently from the computer. These software routines are also capable of reading the real-time beam data stored in the on-board DDR3 memory. These data are displayed on the screen and saved on the local disk for analysis.

The FPGA hardware can be configured in two working modes: operational mode and research mode. In operational mode, the FPGA board captures data from the pickup, processes the data and feeds it back to the kicker. In parallel, a LabVIEW routine monitors the power amplifiers for faults and stops the FPGA boards if any amplifier faults occur. The software routine also monitors the system gain on the FPGA to make sure that the feedback system is within the linear dynamic range of the DAC. It also notifies the user if saturation occurs in any of the internal multipliers.

In research mode, a LabVIEW routine is synchronized by the trigger to fetch the real-time data from the DDR3

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memory. A single-error correcting and double-error detecting (SECDED) coding module is used to correct bit errors that occur when storing the data in memory and transmitting them via Ethernet.

CONTROL SYSTEM RESPONSE

The closed loop feedback damper response is shown in Figure 3. The transfer function of this response is expressed in Equation (1):

$$\frac{Y(s)}{R(s)} = \frac{G(s)}{1+G(s)H(s)} \quad (1)$$

In this equation, *H(s)* can be simplified as a second order system. *G(s)* is unknown and is a high-order nonlinear time-variant system that can be simplified as a stationary stochastic process. With *L(s)=G(s)H(s)*, it is required that all the zeros of *L(s)* are in the left-half s-plane to get a stable closed loop feedback damper system [5].

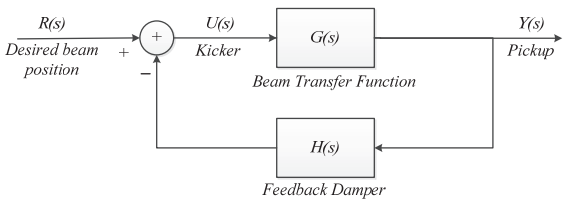

Figure 3: Block diagram of response for the feedback damper system.

The transverse beam transfer function (BTF) is obtained by exciting the beam with a time-varying harmonic signal. The ratio of the response to the excitation in the frequency domain is defined as the BTF. A network analyzer supplies the excitation signal to the kicker and acquires the response signal from the pick-up. Figure 4(a) and (b) show the BTF magnitudes for the horizontal and vertical planes.

The horizontal axis of Figure 4 is the tune, the vertical axis is the mode (the harmonic number of the ring frequency), and the color-bar is the magnitude of the BTF in dB. The side bands clearly show the individual tunes for each transverse plane, with a horizontal tune of 0.225 and a vertical tune of 0.168. The side bands of both planes start diverging into two branches at about the 30th mode and end at about the 150th mode.

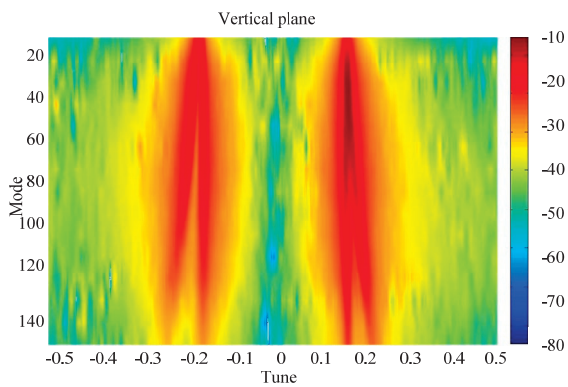

Figure 4(a): The magnitudes of the BTF for the vertical plane.

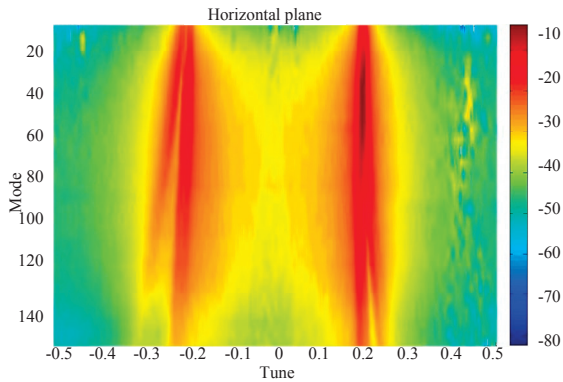

Figure 4(b): The magnitudes of the BTF for the horizontal plane.

Studies are currently being conducted to examine the effects limiting the damping rate and its stability. Studies are also exploring the divergence of BTF to reveal its relationship with the betatron tune.

CONCLUSION

To ramp up the power and mitigate the instability in the SNS accelerator, we implement a wide-band, mixed-signal feedback damper system. The system consists of one FPGA card and a LabVIEW workstation. Several experimental studies have been carried out to understand the system performance and its limitations. The next step is to commit the system and perform physics studies.

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