USE OF FPGA-BASED CONFIGURABLE ELECTRONICS TO CALIBRATE CAVITIES

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Abstract

At the GSI Helmholzzentrum für Schwerionen-forschung GmbH the accuracy requirements for synchrotron rf cavities have strongly increased in the last years, especially for multi-harmonic operation. For heavy-ion acceleration the amplitude and phase have to be well adjusted over a whole machine cycle. In order to compensate small deviations induced by low-level rf components (LLRF) and transmission lines in the control paths, a calibration electronic (CEL) with a characteristic map was developed. It is a real-time module which is based on modern FPGA (Field Programmable Gate Array) technology and adaptable to special cavities with various physical dependencies (e.g. attenuation, dispersion, temperature drift, aging etc.). The hardware and software architecture of this CEL module are presented here.

INTRODUCTION

In the next years, the new international accelerator facility FAIR (Facility for Antiproton and Ion Research), will be established at GSI. At FAIR, a variety of experiments will be possible [1], [2]. Several new synchrotrons and storage rings will be built. The existing heavy-ion synchrotron SIS18 (SIS denotes "Schwerionen-Synchrotron," heavy-ion synchrotron) has to be upgraded to serve as an injector for the FAIR accelerators. All this entails new requirements for the LLRF-systems*. Since 2002, a completely new system architecture has been developed at GSI in order to fulfil these tasks [3]. The new LLRF system will be used for the existing machines SIS18 and for the experimental storage ring (ESR) as well as for the FAIR synchrotrons [2]. Closed-loop control systems that stabilize the amplitude and the phase of the rf gap voltages are used in the LLRF system. This stabilization, however, is not perfect because of a non-ideal frequency response of several components. Accuracies of better than ±6 % for the amplitude and ±3 ° for the phase are required in order to reach the desired beam quality. This demand of accuracy has to be reached under dynamic conditions, i.e. during acceleration. A CEL module was developed in order to reach these requirements. The CEL module adjusts the set values provided by the central control system (CCS) in such a way that the inaccuracies of the transmission paths and errors of inserted components are compensated. The amplitude of the rf gap voltage error depends on both the operating frequency (frequency response) and the modulation amplitude (linearity error). For the phase, the correction depends on the frequency only.

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* In detail, these requirements include: fast ramping modes, arbitrary ion species, and complex beam manipulations such as dual-harmonic operation, bunch compression, bunch merging/splitting, and barrier bucket operation.

HARDWARE IMPLEMENTATION

The CEL hardware consists of a FPGA-interface board (FIB) [4] and a FAB-ADC/DAC extension board [5] in a 19'' frame-type plug-in unit depicted in Fig. 2. The FIB is a multi-purpose printed circuit board (PCB). An FPGA selected from Altera's cyclone family is used as a central component. Several interfaces have been standardized (e.g. four optical links are available which may be used as an optical direct link (ODL) or as an optical token ring (OTR) [6] and a backplane connector can be used to receive and send information to the central control system). The FAB-ADC/DAC board (see Fig. 1), an additional extension board, is linked via dedicated connectors with the FIB. It mainly consists of two ADCs (14 bit up to 125 MSPS), an Altera Cyclone III FPGA, and two DACs (14 bit up to 210 MSPS).

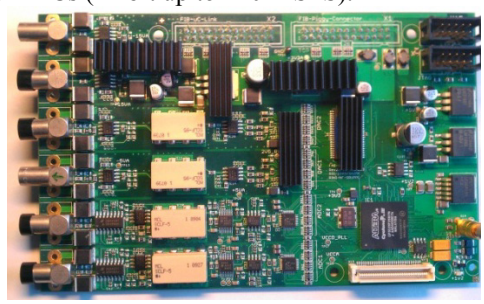

Figure 1: FAB-ADC/DAC extension board.

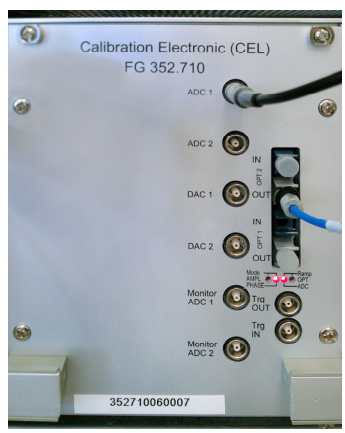

Figure 2: CEL module.

FIRMWARE DESIGN STRATEGY

Network-on-Chip (NoC)

A VHDL (very high speed integrated circuit hardware description language) library was created. This library includes pre-programmed and reusable VHDL modules (e.g. various subsystems and modules for accessing different types of interfaces). All these modules are equipped with a standardized Network-on-Chip interface called FPGA universal bus (FUB) [7] for interconnection on FPGA level. Complex software can easily be built up by composing different modules.

Multirate Signal Processing

The cut-off frequency of the anti-aliasing filters is 5MHz. Since the necessary bandwidth of the CEL module is DC to 100 kHz (see. Table 1), the signal of interest can be found in a much smaller frequency band. Therefore, a multirate signal processing system, described in [8] was designed. Two different types of cascaded-integrator-comb (CIC) filters are required (upper left and right corners in Fig. 3). The first CIC filter (decimator) reduces the sampling rate down to the Nyquist rate ($f_{S,down}$=250 kHz) after the analogue-digital-conversion. A second CIC filter (interpolator) increases the sampling rate up to the clock frequency ($f_{S,up}$=100 MHz) of the digital-analogue converters (DAC). The benefits of a multirate signal processing system are:

- Clock rate reduction of the DSP structure which leads to much lower power consumption of the FPGA.
- Improvement of the SNR (signal-to-noise ratio) due to the bandwidth limitation and an increased bit resolution of the ADC input stream.

Table 1: Electrical Characteristics of CEL

Parameter	Value
Analogue input/output range	-10 V … +10 V
Digital frequency input/output via optical links[6]	0 to 200 MHz Resolution: 47 mHz
Overall accuracy	< 1 %
Offset error	< 10 mV
Low-frequency bandwidth	DC to 100 kHz
Propagation delay	< 60 µs

Digital ADC/DAC Calibration

An ADC/DAC-calibration subsystem is required in order to meet the accuracy requirements and offset errors specified in Table 1. This subsystem consists mainly of 16-bit fixed-point pipelined adders and multipliers to remove linear offset and to gain errors. This subsystem adjusts the digital output stream of the ADCs/DACs continuously, using the equation:

$$output = GCC \cdot input + OCC\,. \qquad (1)$$

A sequence control for the power-up calibration as well as for the online calibration is provided on the FPGA to determine the gain calibration constant (*GCC*) and the offset calibration constant (*OCC*). A monolithic switch is used to connect a voltage reference source, a ground signal, a DAC output or a signal input to the ADC input during the automatic calibration process.

Fixed-to-Floating-Point Converter

In order to increase the accuracy of the subsequent processing steps, a fixed-to-floating-point converter transforms the 16 bit fixed-point data into 32 bit floating-point single precision format according to IEEE 754. All floating-point data are scaled to SI base units.

Floating-Point Arithmetic Unit (FPU)

The input values for the FPU are the pre-processed ADC input values and the interpolated correction values supplied by the characteristic map subsystem refer to chapter Characteristic Map Subsystem (CM). The ADC input can be multiplied by a correction value or the correction value can be added based on a floating-point format.

Fiber-Optic Transmitter and Receiver

Four optical links (low cost fiber-optic transmitters operating at 650 nm wavelength) are available on FIB for input/output of digital values via ODL. A Manchester encoding/decoding-algorithm is implemented directly on the FPGA. Streaming data (ramps) such as frequency, voltage, and phase ramps are received or transmitted via these optical links. All optical data are converted according to IEEE 754 and scaled to SI base units on FPGA level.

Characteristic Map Subsystem (CM)

A 3D characteristic map (CM) composed of floating-point nodes is stored in a random-access memory (RAM) on the ADC/DAC-FAB [9] (see Fig. 4). The CM subsystem has two input ports which correspond to the x- or y-axis of the CM. The output is an interpolated z-value. Two independently working search algorithms (x- axis and y-axis) are required to find the corresponding interval on the x- or y-axis intercept. One of the main objectives was to implement a fast search algorithm with a moderate consumption of resources. An exclusive and a fast memory access is crucial for independently working search algorithms. Therefore, two additional high-speed RAM modules are installed on the FPGA. The control unit initialise these RAM modules with a copy of the x- and the y-axis floating-point nodes respectively. The evaluation of inequalities, based on floating-point values is very efficient on FPGAs. Using the bisection method [10], one gains a powerful and efficient search algorithm. The delay time for obtaining a result is constant and only determined by the number of nodes on the corresponding axis. The delay time in clock cycles can be calculated by:

$$\Delta T_{clks} = \log_2(\text{Number of Nodes}). \qquad (2)$$

The real-time capability of the search algorithm is guaranteed by the high clock rates on modern FPGAs and the constant delay time of the search algorithm.

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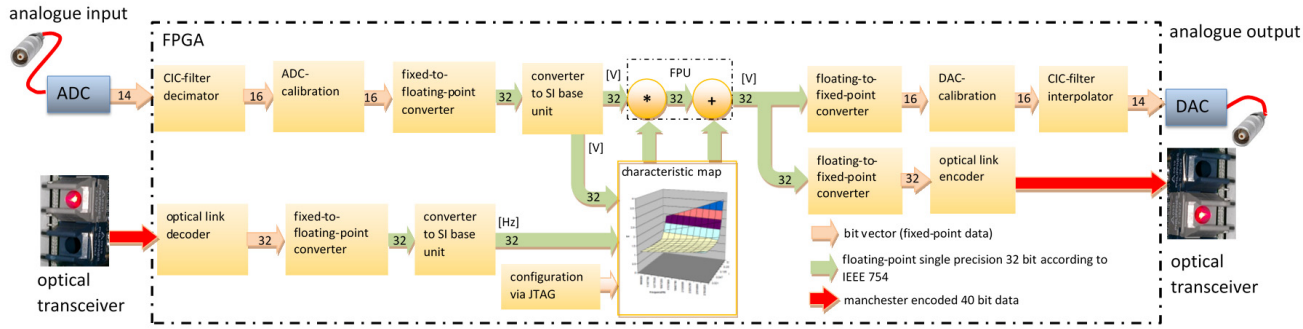

Figure 3: Block diagram of the CEL-electronic.

An interpolation module (see Fig. 4) was implemented to calculate a more accurate z-value resulting from the four adjacent z-value nodes in order to smooth small discontinuities. Depending on the accuracy requirements, several interpolation methods are available.

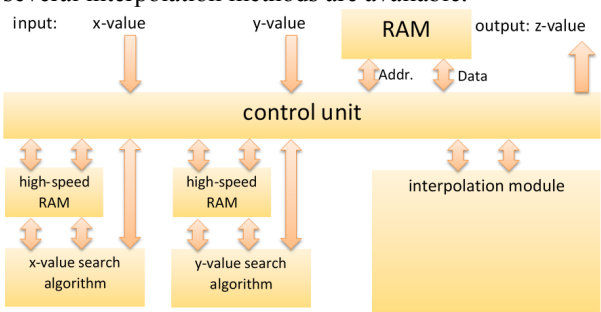

Figure 4: Block diagram of the characteristic map.

DEBUNCHING EXPERIMENT IN SIS18

Four CEL modules were installed in the SIS18 LLRF system (one for the amplitude and one for the phase for each of the two cavities). Calibration maps depending on the frequency and the amplitude were automatically measured and loaded into the CEL modules. During the beam experiment [11], [12] both cavities operated with opposite phase (180°) but with the same amplitude. In case of a perfect calibration, a debunched beam was observed. The experiment has shown that the required accuracy of ±3 ° for the phase and ±6 % for the amplitude can be clearly fulfilled.

CONCLUSION AND OUTLOOK

In the scope of FAIR@GSI the accuracy requirements for synchrotron rf cavities have strongly increased in order to reach the desired beam qualities. A calibration electronic (CEL) was developed in order to reach these accuracy requirements. Calibration fields stored in a 3D characteristic map are used to adjust the set values provided by the central control system in real time. A beam experiment [11], [12] in the SIS18 has shown that the required accuracies of better than ±3 ° for the phase and ±6 % for the amplitude under dynamic conditions are achieved without difficulty. The CEL module opens a wide range of applications at GSI. In future, CEL modules will improve the accuracies of different control systems (closed-loop or open-loop) and of the LLRF components (e.g. phase response of a DDS module). It is possible to correct different kinds of errors like offset-, gain- or linearity-errors resulting from various physical dependencies. A reliable operation requires a reproducibility of these errors (at least temporarily).

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