LLRF SYSTEM FOR LCLS-II AT SLAC*

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Abstract

After LCLS-I successfully delivered the full operation for users, SLAC was approved to build the second Linac Coherent Light Source, LCLS-II, which makes use of another third of the 2-mile long Linac from Sector 10 to Sector 20. The LLRF System will replace the VME crate with MicroTCA (Micro Telecommunication Computing Architecture) for LCLS-II injector and some key stations along the LINAC. The faster data acquisition and more powerful FPGA and CPU available in the MicroTCA system enable the LLRF system to extend its control ability to a 2.5 µsec beam pulse at rate of 120 Hz. The new LLRF system is more compact and has the capability of low latency intra-pulse feedback to reduce fast phase and amplitude jitter during a single pulse. The prototype of the MicroTCA based LLRF control system has been operating at RF station 28-2 in LCLS-I. Detailed design structure and the prototype experimental results will be presented that demonstrate the system meets the requirements of LCLS-II.

INTRODUCTION

LCLS-II is primarily modelled after LCLS-I design with selected modifications and enhancements. The LCLS-II structure is shown in Fig. 1. The high beam stability for FEL generation requires RF phase and amplitude to be within the tolerances shown in Table 1 for each section of the machine.

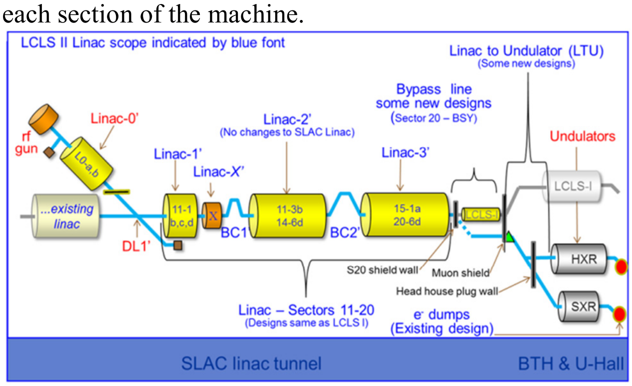

Figure 1: LCLS-II Structure Layout.

The LLRF system provides the synchronized RF reference to the Drive Laser System, Timing System and its own sections from the Injector to the LINAC. The phase and amplitude jitter for all signals must meet the stringent requirements defined in the LCLS-II Physics Requirement Document [1]. The LLRF system will measure the RF signals, control the RF power sources and act as RF actuators for the Fast Feedback System. Special RF cabling is installed to ensure reliable and high quality RF connections between the RF sources, controller, detectors and high power devices. The major parts of the LLRF control instrumentation are located inside the temperature controlled enclosures.

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Table 1: RF Stability Requirements for LCLS-II

Parameter	Symbol	tolerance	unit
Drive-laser timing error	Dt	0.20	psec
L0 RF phase error	Df_0	0.10	degS
L1 RF phase error	Df_1	0.07	degS
LX RF phase error	Df_x	0.50	degX
L2 RF phase error	Df_2	0.05	degS
L3 RF phase error	Df_3	0.30	degS
L0 RF rel. amplitude error	DV/V_0	0.07	%
L1 RF rel. amplitude error	DV/V_1	0.06	%
LX RF rel. amplitude error	DV/V_x	0.25	%
L2 RF rel. amplitude error	DV/V_2	0.07	%
L3 RF rel. amplitude error	DV/V_3	0.10	%

LLRF HARDWARE SYSTEM

The overview of the LCLS-II LLRF Control System [2] [3] is shown in Fig. 2. Tapping off from the Main Drive Line, the Frequency Reference Subsystem in Fig. 3 generates the 476MHz, 2856MHz and 11.424GHz references; 68MHz, 119MHz and 102MHz clocks; 2830.5MHz and 11.3985GHz LO signals with respect to 2856MHz S-band RF and 11.424GHz X-Band RF signals. These signals are distributed to the LCLS-II Injector and LINAC. The measured integrated noise of 2856MHz and 2830.5MHz from 10Hz to 10MHz are <30fs.

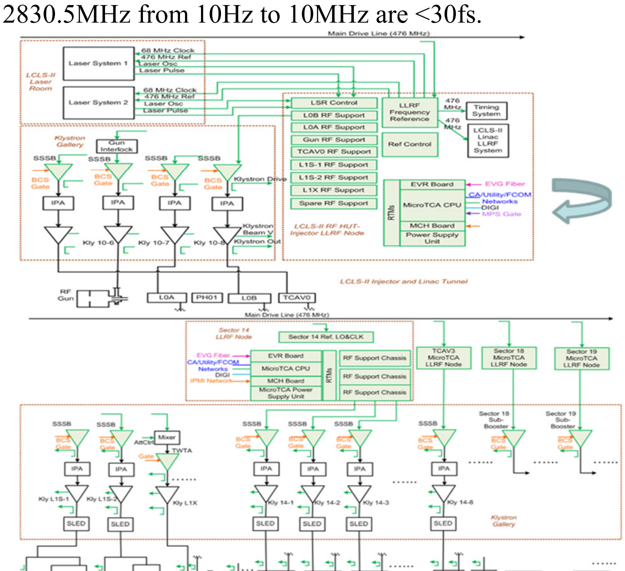

Figure 2: The overview of the LCLS-II LLRF Control System.

Slow Phase and Amplitude Controllers (SPACs) are used to adjust the phase relationship between different sections of the subsystems. See Fig. 3. The lower frequencies, such as 25.5MHz, 68MHz, 119MHz and 476MHz are directly sampled by high bandwidth ADC channels and their phase and amplitude calculated by software using digital demodulation algorithms. The 2856MHz and 11.424GHz RF signals are down-mixed to 25.5MHz and then sampled by ADCs.

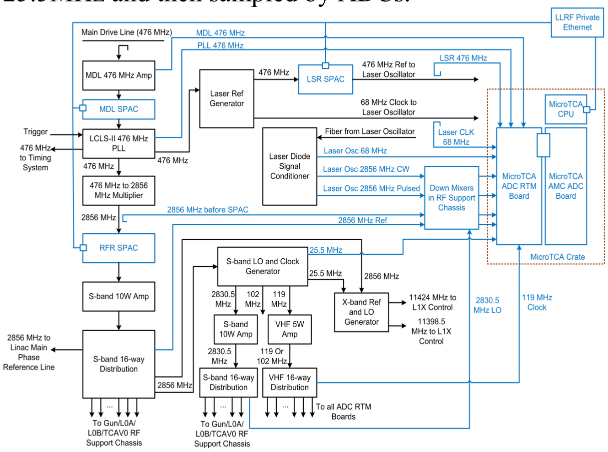

Figure 3: LLRF Frequency Reference Subsystem [2].

For each Drive Laser Oscillator, a Laser Diode Signal Conditioner is added to derive the basic harmonic (68MHz) and the 42th harmonic (2856MHz) of the diode signal from the laser pulses. Both signals are measured for laser timing diagnostics with different resolutions.

All four of the Klystron RF stations in the Injector, L1, LX and parts of the L2 and L3 stations will be upgraded to have individual phase and amplitude control with MicroTCA controllers and Solid State Sub-Boosters (SSSB) working as fast phase and amplitude actuators for 120Hz pulse-to-pulse control, possible intra-pulse stabilization and beam energy control. Fig. 4 shows the architecture of a typical Klystron Station control for LCLS-II. [4]

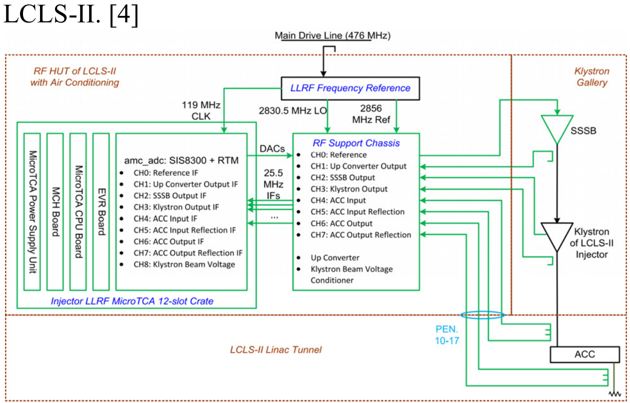

Figure 4: Architecture of a typical Klystron Station Control.

For each klystron, an RF Support Chassis is created to package the analog signals for RF controls. It consists of 8 channels of down mixer channels, 1 channel of up converter channel and 1 Klystron Beam Voltage conditioner. In the MicroTCA crate, an AMC ADC board is used to measure the down mixed IF signals, to perform feedback control, and generate DAC outputs to drive the up converter. The RF signals from different locations of the klystron station and the klystron beam voltage signal are fed into the RF Support Chassis to be down mixed and conditioned. An SSSB amplifier installed in the klystron gallery amplifies the modulated RF signal from the up converter to around 1kW to drive the klystron. The RF Support Chassis with down-mixer and up-converter modules are shown in Fig. 5.

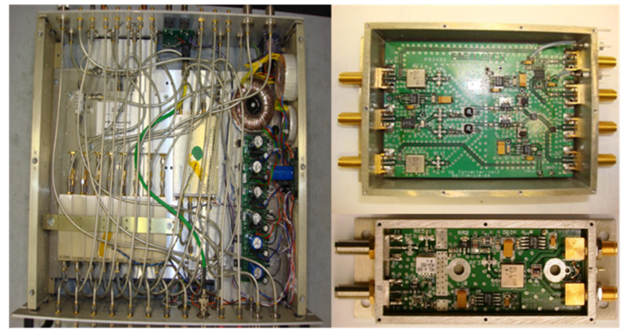

Figure 5: The RF Support Chassis (left) with Up Convert (right-up) and Down Mixer Modules (right-bottom).

THE MICROTCA SUBSYSTEM

The MicroTCA based design is more compact and offers a robust system architecture with significant increases in computational real-time processing power and data transfer performance. This enables improving RF stability by introducing intra-pulse feedback for both amplitude and phase control. Simplified system architecture and built-in redundancy features of MicroTCA improve the reliability of the system. The cost of MicroTCA based design is comparable with PAD/PAC based design [5], but with much lower maintenance cost during system operation.

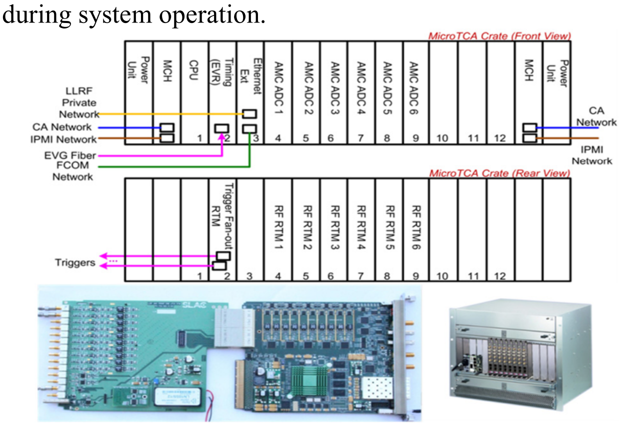

Figure 6: 12-slot MicroTCA Crate for LCLS-II Injector LLRF and AMC-ADC Board-Struck SIS8300 with SLAC RTM.

Fig. 6 shows a 12-slot MicroTCA crate with 6 AMC ADC boards in it. This structure will be used to collect most of the digital hardware for LCLS-II Injector LLRF system. A Struck SIS8300 board interfaced with a SLAC designed RTM also shown in Fig. 6 was selected as the AMC ADC board; it features 4-lane PCI Express; 10 Channels of 125MS/s 16-bit ADC; two 16-bit DACs for Fast Feedback implementation; twin SFP Card Cage for High Speed System Interconnects and a Virtex 5 FPGA.

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FIRMWARE/SOFTWARE SYSTEM

The top level architecture of the LLRF firmware/software is described in the block definition diagram in Fig. 7.

A general and configurable firmware is designed as the fast controller for the RF stations of LCLS-II, see Fig. 8. The firmware is installed in the FPGA of the SIS8300 board. It implements the fast real-time functions for the RF station control, including I/Q demodulation of the RF signals, intra-pulse phase and amplitude control (measure the error from the first part of the 2.5µs RF pulse and apply the correction on the last 1µs of pulse for beam acceleration), RF pulse generation and the calibration of the I/Q modulator. The firmware data acquisition module supports acquiring 64K samples on 10 ADC channels at a 125MSPS sampling rate, enabling the SIS8300 board to be used as a general digitizer.

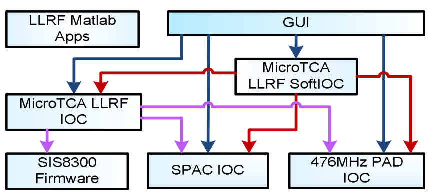

Figure 7: Architecture of the LLRF firmware/software.

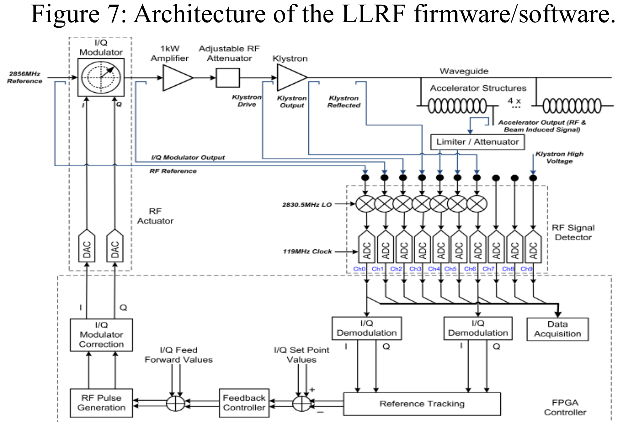

Figure 8: Architecture of the LLRF Firmware.

EPICS is the control platform for the LLRF software. The real-time component of the LLRF software (MicroTCA LLRF IOC) will be installed in the MicroTCA CPU. This processor is running real-time Linux to fully support 120 Hz operation; including pulse-to-pulse feedback, fast beam based feedback and beam synchronized data acquisition. A soft IOC (MicroTCA LLRF Soft IOC) performs many of the slow control functions within the LLRF system, like calibrating the I/Q modulator, configuring LLRF firmware and the automation procedures for the LLRF operation. The Matlab applications, like the resynchronization of the frequency generator and phase jitter calculation, will be immigrated to LCLS-II LLRF. Comparing to LCLS-I LLRF system, the new GUI is more user-friendly and the users' panels and the experts' panels will be well separated. Fig. 9 shows the users' panel for the RF station top level control.

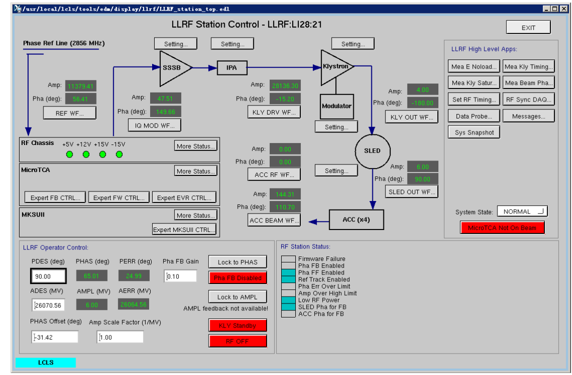

Figure 9: Users' Panel for RF Station Control.

PROTOTYPE TEST RESULTS

The prototype of the MicroTCA based LLRF system has been demonstrated at SLAC Klystron RF Station 28-2 for LCLS operation. The pulse-to-pulse feedback could effectively remove the low frequency (<10Hz) phase fluctuations [2]. The intra-pulse feedback based upon the measurments showed that the fast phase jitters can be reduced by about 20% [2]. The prototype was succesfully deployed to beam operation and its GUIs received praises from the physicists and operators alike. More test results such as RF station phasing are shown in Reference [2].

CONCLUSION

The MicroTCA based platform has been proven to be a valuable technology to support RF control systems. A prototype of the MicroTCA LLRF system has been developed, tested and deployed. It has proven to provide better performance, improved RF stabilities, and increased robustness and reliability when compared to the exisitng PAD/PAC based LLRF system used in LCLS-I. The MicroTCA architecture has been officially adopted for the LCLS-II LLRF and BPM systems.

ACKNOWLEDGEMENT

The LCLS-II LLRF system design is based on the LCLS-I LLRF System, for which Ron Akre was the major designer. He built the foundation of reliable LLRF control for LCLS-I that was used as the cornerstone for many of the LCLS-II improvements. Ron tragically passed away in 2012. His contributions to LLRF in accelerator society will be always remembered and appreciated.

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