FAST ORBIT FEEDBACK SCHEME AND IMPLEMENTATION FOR TAIWAN PHOTON SOURCE

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Abstract

TPS (Taiwan Photon Source) is a 3 GeV synchrotron light source which is being in construction at NSRRC. As most of 3rd generation light sources, the fast orbit feedback system would be adopted to eliminate various disturbances and improve orbit stability. Due to the vacuum chamber material made of aluminium with higher conductivity and lower bandwidth, both of slow and fast correctors will be used for FOFB correction. In general, there are two schemes to operate these hybrid correctors. One is to transfer correction from fast to slow correctors periodically and avoid fast corrector saturation. The other is the fast correctors operated only at higher frequency domain and slow ones take care of DC part. TPS would adopt the first scheme but the second one still as a substitute. Both schemes will be supported. This report summarizes the infrastructure of the FOFB and the simulation is also presented.

INTRODUCTION

The TPS is a state-of-the-art synchrotron radiation facility featuring ultra-high photon brightness with extremely low emittance [1]. This synchrotron machine requires beam position stability less than 1/10 beam size therefore the FOFB is also required to stabilize orbit and achieve one hundred or even tens of nanometer resolution. The FOFB is mainly implemented by three parts: BPM, feedback computation unit and corrector power supply control interface. The TPS BPM electrical system will adopt the latest I-tech product: Brilliance+ [2] and its acceptance test for all units had been completed during June to August of 2012 to verify to meet fundamental specifications and functionalities. It also offers a large playground for custom- written applications with Virtex 6 in the gigabit data exchange module (GDX) to be used as orbit feedback computation. The corrector power-supply controller (CPSC) is designed for FOFB corrector control interface. This module is embedded with Intel XScale IOP and Xilinx Spartan-6 FPGA which will interface the fast setting from feedback engines. It was contracted to D-TACQ [3].

THE BPM AND GDX INTERFACE

The BPM electronics consists of four kinds of modules: The timing module for clock locking and trigger; up to four BPM modules for receiving button pick-ups and signal processing, the inter-connection board (ICB) module for SW and HW interface; the GDX (Gigabit data exchange) module for FA data grouping and FOFB computation.

Preliminary BPM testing

Fig. 1 shows the histogram of horizontal and vertical position SA resolution distibution at power level around -10 dBm for 228 BPM modules. Most of these modules could achieve 20 nm resolution.

For turn-by-turn data, the resolutions are 150 for 0.5 mA and 10 um for 10 mA respectively. FA data resolution is around 100 nm for 100 mA.

The current, filling pattern and temperature dependency are also verified. Current dependency is less than 200 nm for 40 dB input power level changes. Different camshaft mode filling patterns are tested to observe position almost not changed (<<100nm). Additionally, temperature dependency are smaller than 100 nm/°C [4].

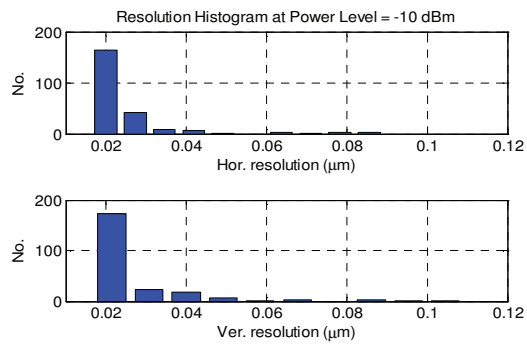

Figure 1: Histogram of horizontal and vertical position resolution distibution at power level around -10 dBm for 228 BPM modules.

Preliminary GDX testing

To verify whether FOFB functionalities on GDX work properly, the preliminary test environment is setup as Fig. 2. The power-adjustable signal generator is applied to three pick-up buttons so that the power setting change will result in three buttons strength change and simulate the corrector magnet causing BPM position change. The result is shown as Fig. 3. It was observed that the position flowed along with the reference orbit which changed between -500, 0 and 500 um. The larger Ki causes the larger overshoot compared the lower Ki.

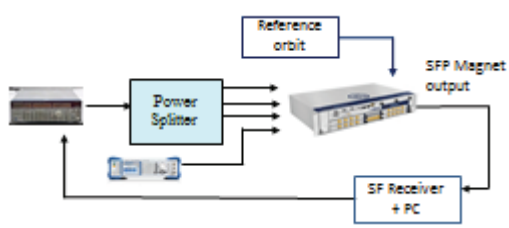

Figure 2: GDX testing setup.

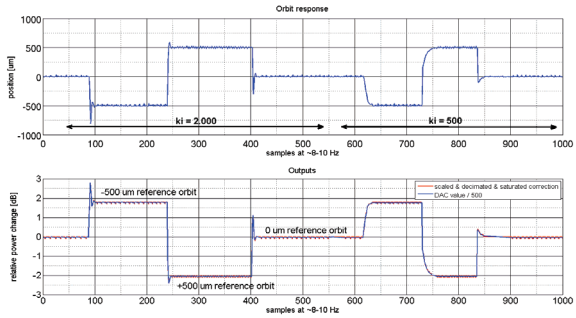

Figure 3: FOFB GDX closed loop test. The upper plot is position; the lower plot is relative power level change.

CORRECTOR POWER SUPPLY CONTROL INTERFACE

The corrector power supply module is a sophiscated switching power supply with analogue regulator [5]. It will be applied for slow correctors, fast correctors, skew quadrupoles and etc. Each power suply sub-rack accomodates up to eight power supply modules. The center slot is allocated to install a special designed EPICS IOC with feedback support.

The corrector power-supply controller (CPSC) module is embedded with ARM processor and Xilinx Spartan-6 FPGA. It was contracted to D-TACQ. This module will be installed at center slot of the power supply sub-rack. The module embedded EPICS IOC and FPGA supports slow access for the EPICS CA clients and fast settings from orbit feedback system or the feedfoward application such as skew compensation. The fast settings from feedback engines with rocket I/O or feed-forward engines with Gigabit ethernet will be sumed together with slow settings in CPSC to regulator module of corrector. The functional block diagram of CPSC module is shown in Fig. 4.

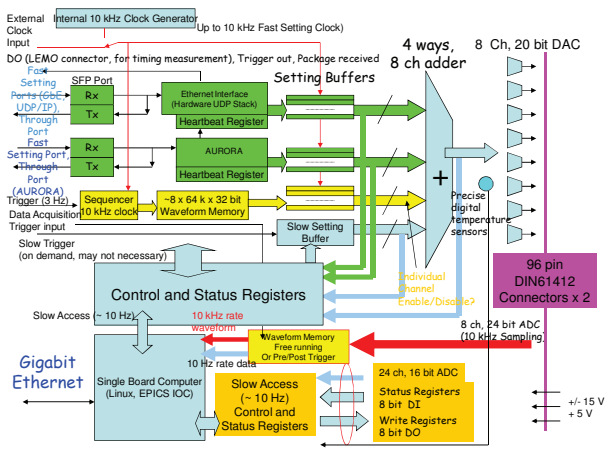

Figure 4: Functional block diagram of the corrector power supply controller module. Fast setting from orbit feedback and slow setting from EPICS CA console.

Preliminary corrector power supply testing

The power supply achieves 20 bit performance where it is equivalent to 1 nrad resolution for slow corrector control and 0.05 nrad for fast ones. Noise level is around -120 dB where it would contribute 200 nm RMS orbit disturbances from total 168 slow correctors and 10 nm for 96 fast correctors. Compared to slow correctors, orbit disturbance cause by fast correctors could be ignored. Furthermore, the fast corrector response is corresponded to the 1.3 kHz bandwidth. The test results are shown as Fig. 5.

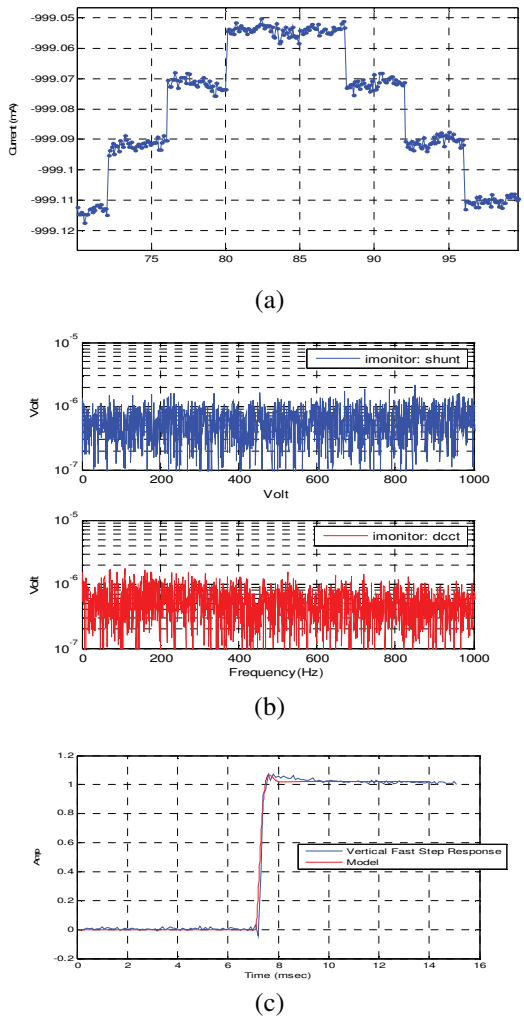

Figure 5: (a) 20 bit performance, each step is around 20 uA. (b) Noise level is around 1uA (c) Step response of vertical corrector power supply.

FAST ORBIT FEEDBACK WITH SLOW CORRECTOR COMPENSATION

The lattice layout for one cell of TPS storage ring is as Fig. 6. There are 7 BPMs and 7 horizontal/vertical correctors are winding on the sextupoles in each cell to provide hundreds of micro-radian kick strength while their bandwidth could be limited much less than 100 Hz due to the TPS alumni vacuum chamber. Therefore, extra four fast horizontal/vertical correctors are installed on the bellows which have fast response but smaller trim strength around 20~30 urad [6]. The fast corrector will be used for feedback correction to suppress various

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disturbance form DC to 300 Hz. Another process will have to check the fast corrector setting periodically and transfer DC part setting to the nearby slow correctors when accumulating to avoid saturation. FOFB integration test will be possible in 2014.

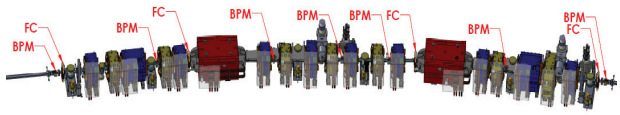

Figure 6: One cell of 24 double-bend cells for TPS lattice layout.

Simulation result

Static simulation for vertical FOFB is performed as Fig. 7. It is assumed the random noises including qaudrupole 1 um displacement and slow corrector 100 nrad noise and then acquires σ_y from 200 simulation results. The amplify factor would cause average 40 um orbit displacement without FOFB while the orbit displacement could be suppressed less than 1 um when applying FOFB. See Fig. 1, the upper plot selects all of 7 BPMs in one cell; the lower plot selects only 5 BPMs in one cell where it results in larger displacement in bending section while the straight line displacement still could achieve 300 nm stability.

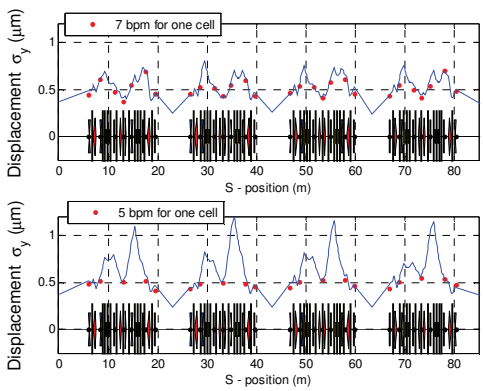

Figure 7: Static simulation for FOFB shown in 4 cells.

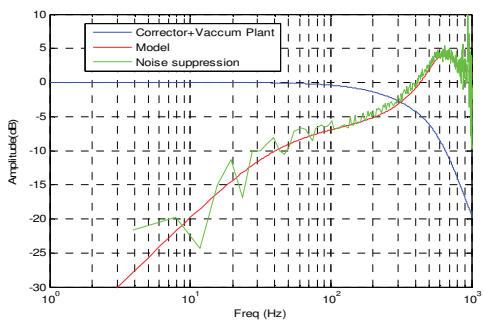

Figure 8: Simulation of noise sensitivity function of the FOFB system.

The bandwidth of the FOFB to suppress noise is estimated around 300 Hz which is limited primarily by corrector and chamber. The simulation result is shown in Fig. 8. The noise amplification effect will occurs at 600 Hz far away from major noise spectra.

Fig. 9 shows the transaction when DC part of fast corrector transfer to slow corrector. At 50 msec, a kick cause orbit excursion and soon FOFB suppress it in 10 msec and it results in one corrector (fast VC011) has 60 mA DC offset. At 100 msec, the nearby slow (slow VC011) take DC parts of the slow correctors and fast corrector decreasing to zeros. The transaction between slow and fast will only cause orbit disturbance less than 1 um and vanish in 10 msec.

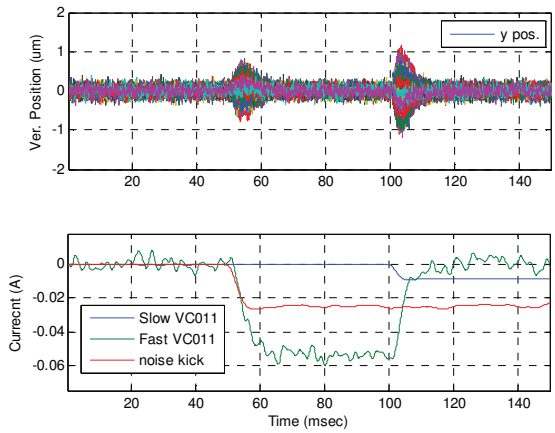

Figure 9: Transaction simulation when the fast corrector DC setting is transfer red to the nearby slow corrector.

CONCLUSION

BPM electronics and fast orbit feedback system combined with slow and fast correctors of the TPS are summarized. The BPM electronics completed acceptance test in 2012. CPSC will be delivered in 2013. Preliminary tests for done. Installation and system integration will be performed in early 2014. Platform development is also on going to develop various software supports.

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