PROGRESS ON THE ISIS SYNCHROTRON LOW POWER RF SYSTEM UPGRADE

A. Seville, D.B. Allen, D.L. Bayley, N.E. Farthing, I.S.K. Gardner, W. Huang*, R.J. Mathieson,
STFC, Rutherford Appleton Laboratory, Chilton, Didcot, UK.
*IHEP, Beijing, China.

Abstract

The ISIS synchrotron at the Rutherford Appleton Laboratory in the UK now routinely uses a dual harmonic RF system to accelerate beam currents in excess of 230μA to run two target stations simultaneously. In order to give more stable control of the phase of the RF voltage at each of the fundamental (1RF) and second harmonic (2RF) cavities, changes have been made to the low power RF (LPRF) control systems. A new FPGA based master oscillator has been implemented using a National Instruments FlexRIO FPGA module. This has allowed a relatively rapid deployment for various modules and functionality of the LPRF system, including a replacement master oscillator, which has now been commissioned with beam for the first time. This paper reports on the commissioning of the FPGA master oscillator (MO) and plans for the gradual replacement of remaining parts of the LPRF system.

INTRODUCTION

The ISIS LPRF system has been used successfully to accelerate beam on the ISIS synchrotron for the last 30 years. Recent changes to the LPRF system have been implemented, including the addition of multipliers in the level control loops to maintain constant gain, and increase stability of the cavity gap voltages. In recent ISIS user cycles, three 2RF cavities have been used to provide dual harmonic acceleration rather than the two cavities used previously. This has enabled the gap voltages on each cavity to be lowered and subsequently the cavity liquid resistors have been reduced from ~5kΩ to ~2.5kΩ. This in turn has reduced the effects of beam loading on the cavities and, together with the increased RF system stability, has allowed the prospect of operation with four 2RF cavities for first time in the next ISIS user cycle.

The LPRF system is used to generate and control the amplitudes and phases of the RF voltages and also to maintain tuning of each of the ferrite loaded RF cavities during the 10ms frequency sweep of ISIS acceleration. Much of the technology is now becoming dated. Previous upgrades have been made on the frequency law generator and master oscillator unit [1,2], using an FPGA based approach. The latter consisted of a bespoke unit, which took many years to refine, but did yield promising results. As the power of FPGA devices has increased over the last number of years, it was decided to attempt to implement more of the functionality of the existing LPRF system, shown schematically in figure 1, on such a device.

The availability of the National Instruments FlexRIO series of PXI express based FPGA modules and front end adapters gave an opportunity to utilise 'off the shelf' hardware and in-house Labview programming expertise to produce prototype algorithms for the LPRF control system in a relatively short development time. The initial phase of development system consisted of a NI PXIe 1062Q PXI express chassis housing a single NI PXIe 7962R FlexRIO FPGA module and a NI 5781 baseband transceiver module, with dual 14bit 100MS/s ADCs and 16bit 100MS/s DACs. This system is shown in figure 2.

Figure 2: PXI express chassis with FPGA module.

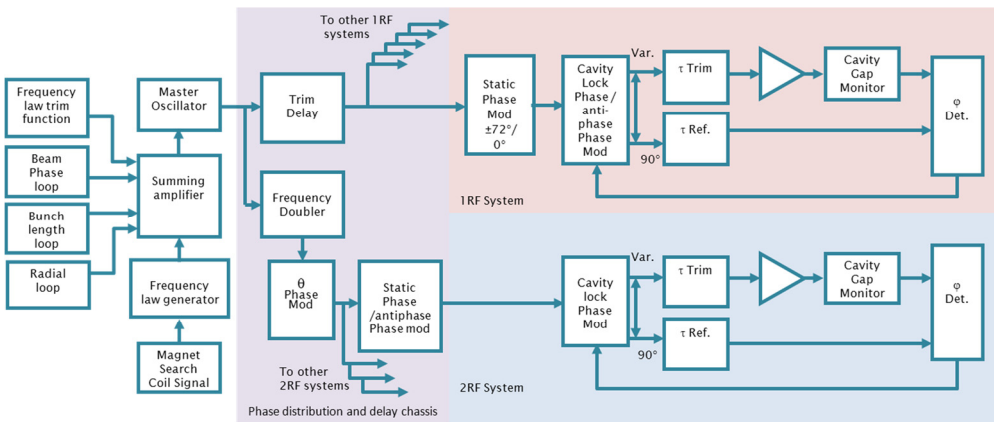

Figure 1: System diagram of the ISIS low power RF.

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The system above was first utilised to replace the VCO based master oscillator. This unit converts the analogue voltage signal from the ISIS frequency law generator summed together with the frequency law trim function and the radial, bunch length and beam phase loops into the main fundamental RF signal.

The algorithm used on the FPGA module digitises the incoming frequency law generator (FLG) summing amplifier output and scales this value to give a variable counter increment used to step through a 65536 location deep, 16bit wide sine-wave look-up table (LUT) implemented using the Xilinx Optimised DDS block RAM. For the fixed 100MHz FPGA clock rate used, the larger the counter increment, the faster the progress through the LUT and therefore the higher the output frequency. A simple doubling of the counter increment can also provide a 2RF sine wave signal. Course delays in each signal can be applied by pipelining of the digital stream by multiples of the 10ns clock cycle. Finer delays are implemented by applying a weighted average of two successive samples, giving sub-picosecond delay resolution. The digital waveform is then output to the 16bit DAC and fed into the phase distribution and delay chassis of the existing system, where it was used to accelerate beam for the first time in November 2012.

MASTER OSCILLATOR BEAM TESTS

The digitiser DC offset and scaling functions were adjusted slightly to match the RF frequency at beam injection and extraction. Initial tests of a low rep rate ISIS beam accelerated by the RF system using the new FPGA based master oscillator looked promising, accelerating 2.5×10^{13} protons of the 2.7×10^{13} injected protons. However the beam stability appeared slightly different from that accelerated using the analogue system. Beam loss signals appeared similar, but the beam appeared to suffer slightly larger oscillations, particularly in mean horizontal position as shown in figure 3.

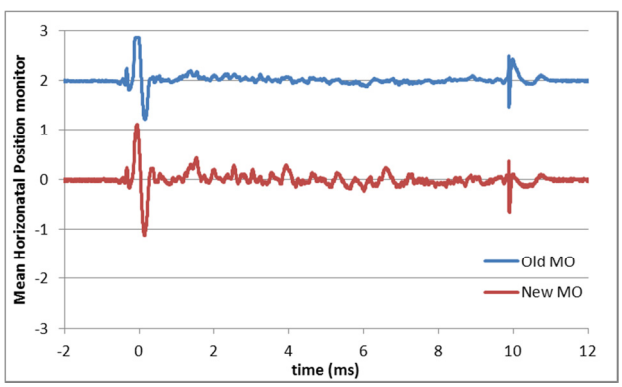

Figure 3: Mean horizontal beam position signal for the Old MO (2V offset) compared with the new FPGA MO.

The regular features in the mean horizontal position signal were thought to be due to limits in the resolution of the digitiser leading to large discontinuities in the instantaneous frequency of the RF system. This was improved by buffering of the summing amplifier output signal to better match the ±1V input level of the digitiser, giving effectively twice the frequency resolution. Beam tests for the improved system were repeated in February 2013. Figure 4 shows the corresponding results for the improved digitiser resolution and figure 5 shows the corresponding beam loss monitor. One can see that the losses, for the single pulse captured at least, appear to be no worse for acceleration with the new MO.

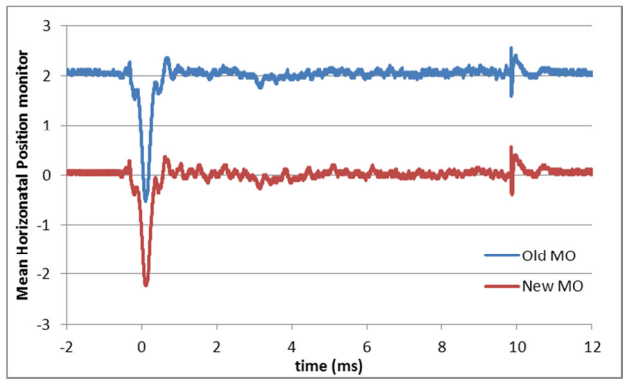

Figure 4: Mean horizontal beam position signal for the Old MO (2V offset) compared with the new FPGA MO with improved input signal buffering.

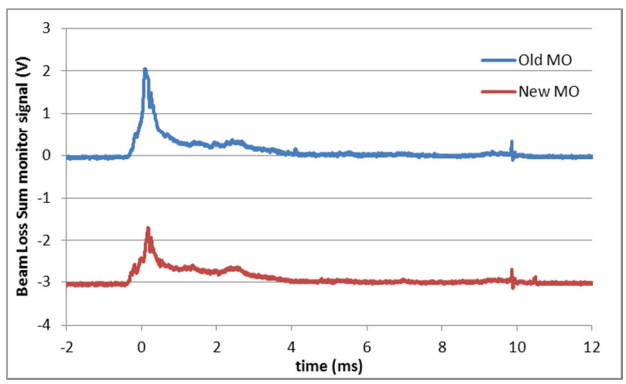

Figure 5: Typical beam loss monitor signals for the Old MO compared with the new FPGA MO (-3V offset).

COMBINED MO / PHASE DISTRIBUTION

The initial test system was expanded by the addition of two more FPGA modules and transceiver front ends to allow generation of the required RF signal for each of the 2RF cavities in addition to a 1RF signal input into the existing fundamental RF control system. In this mode, a single FPGA module is used to digitise the summing amplifier input and generate a frequency increment as before, but in addition to outputting the required RF signal on the local transceiver front end, the frequency increment is also broadcast as a data packet via the PXIe trigger lines to the two slave FPGA modules each acting as a local oscillator for two 2RF systems. Clock synchronisation of the 3 FPGA modules was achieved by distribution of a clock trigger over the trigger lines. The local oscillator sums the received frequency counter increment with a DC offset to the counter increment value

for each RF cavity such that the resultant rolling index to the LUT generates a DC phase offset to compensate for the location in the synchrotron for each specific RF cavity. This system was implemented in March 2013. However tests with beam showed the additional delay introduced by the packetisation over the trigger lines to be too large (~5μs) to support successful operation of the beam phase loop. The next stage to be implemented is replacing the trigger line broadcast with peer-to-peer streaming on the PXIe backplane. This boasts up to 3GB/s data streaming across the PXIe backplane and should, in principle, enable frequency counter increment update rates of the order of 40MHz to each of the ten RF systems and reduced latency of the broadcast packet.

COMBINED FLG / MO / PHASE DISTRIBUTION

A further stage to be implemented is the combination of the frequency law generator and master oscillator LUT. In this case the main magnet search coil signal (dB/dt) is sampled directly into one channel of a NI 5734 4 channel 16 bit digitiser adapter module and a running sum used to give the integral which can be mapped directly to a frequency counter increment via a frequency law LUT. The remaining 3 analogue inputs are used to sample the beam phase loop, radial loop and bunch length loop corrections which are scaled accordingly and summed with the LUT output to give the instantaneous frequency increment counter that is broadcast to the each of the five further FPGA modules. At each of these, the phase offsets and delays are applied and then passed to the two DAC channels to provide the RF drive signal to two RF systems. Coding of the initial stage of the combined frequency law and master oscillator has been completed. The addition of the loop correction signals will soon be added and operational beam tests made later this year.

IQ LOOP CONFIGURATION

The final stage of the LPRF upgrade will see the combined FLG / MO implemented on a single FPGA module with a 4 channel digitiser front end which then streams the frequency counter increment (and phase offset for the 2RF systems) to a FPGA module with transceiver front end adapter module which closes the level control loops, phase control loops and tuning loop: one module for each of the ten RF systems. The FPGA control loop implementation is shown in figure 6.

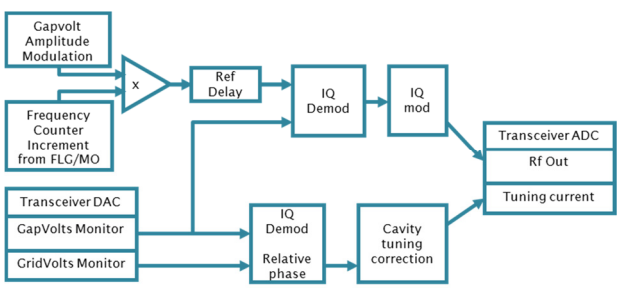

Figure 6: Cavity RF IQ loop and tuning loop implemented on a single FPGA module.

It is intended to combine the amplitude and phase control in a single IQ loop. A similar approach will be used to compare the cavity gap voltage and tetrode amplifier grid voltage to maintain cavity tuning.

IQ demodulation using a single clock cycle multiplier has been implemented along with a low pass decimation filter, giving I and Q values and therefore the relative phase out. The decimation filter used has the advantage of reducing both the latency of the code implementation and FPGA resource utilisation. Code for the IQ modulation is being implemented which will use the I and Q values from the decimation filter to produce the closed loop RF output.

CONCLUSIONS AND FUTURE WORK

The operational requirements of a large scale facility such as ISIS result in limitations on the amount of development time afforded to system upgrades. With this in mind the NI FlexRIO/ PXI express architecture has provided an off-the-shelf platform that has enabled rapid proto-typing and deployment of modular components of, and potentially leading to a deliverable future upgrade of, the ISIS low power RF system.

In the first instance, the implementation of a digital master oscillator on a single FPGA module has now been used to accelerate reasonable beam intensities on the ISIS synchrotron. An 18-slot PXI express chassis and further FPGA modules have been acquired to enable this to be extended to produce a combined digital frequency law generator and master oscillator on one module and then broadcast the instantaneous frequency, via peer to peer streaming, to five other FPGA modules to provide the drive signals for each of the ten RF cavities. The final stage will require further FPGA modules to implement full loop control of the RF voltages and tuning of one cavity on each FPGA module.

Further development and evaluation is required in order to prove the various architectural components for a complete LPRF system, which the FlexRIO module is well suited for. Device resource utilisation for the code implementations made has not been an issue to date. However, alternative hardware solutions are being considered, should a custom system prove to be necessary for optimal performance and operation, which includes a multi-board/multi-FPGA approach or a single system-on-chip (SoC) philosophy. To this end, a Xilinx KC705 Kintex-7 development board with a 250Ms/s ADC and DAC, FMC daughterboard has been purchased, with a view to porting the architectural approaches developed so far across to it, in order for them to be evaluated in this framework.

REFERENCES

[1] C. Appelbee et al, “Digital Master Oscillator results for the ISIS Synchrotron”, PAC’07.
[2] A. Seville et al, “Upgrade of the ISIS low power RF system” IPAC’11.

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