DEVELOPMENT AND APPLICATION OF THE TRIGGER TIMING WATCHDOG SYSTEM IN KEK ELECTRON/POSITRON LINAC

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Abstract

The KEK injector linac provides the different flavors of electron and positron beams to four independent storage rings. The linac beam is injected into the selected storage ring in every time interval of 20 ms since the linac parameters including timing and low-level rf phase can be arbitrary changed up to 50 Hz for the simultaneous top-up injection of three rings. For the achievement of such simultaneous top-up injection, a new event-based timing and control system has been built to change the timing parameters of various linac components less than 20 ms [1]. The components are situated over a 600-m-long linac, and around 200 timing parameters should be stably changed during the long-term beam operation. The new timing system has been operated successfully since the autumn of 2008 and continuously improved upon by a modification of control software. Toward SuperKEKB project, the linac timing watchdog and alert systems are getting important for a day-to-day beam operation since the high available operation system is strongly required. For this purpose, we develop and utilize the several timing watchdog systems. In this paper, we present the detail of timing signal watchdog system for the KEK injector linac in detail.

INTRODUCTION

The linac beam control system comprises the server computers and several front-end computers. Each of them is connected via 1 Gigabit Ethernet control network. In this decade, the server computers have been replaced by a Linux-based one from a Tru64 Unix-based one because of maintenance issue. The original linac control system has been developed by using in-house software libraries based-on the remote procedure calls (RPC). The client user interface has been designed by Tcl/Tk scripts for accelerating software development.

After the KEKB project launched, the linac control system has been upgraded to the framework based-on the Experimental Physics and Industrial Control (EPICS) system to improve the affinity between the ring control systems. For the archiving of around 35000 parameters, both of EPICS Channel Archiver [2] and Control System Studio (CSS) Archiver [3] have been implemented for the linac beam operation. In addition, the newly developed client softwares are designed by Python scripting language for the easy development.

These improvements make it easy to analyze the correlations between the linac and ring parameters. Such analysis is useful to identify the source of injection rate deterioration and so on. Toward SuperKEKB project, the reliability of the timing system together with that of control system is getting important to increase the beam operation availability. For this purpose, the development of the robust timing system is strongly desired. In addition, the development of excellent timing watchdog system is also important. It can be helpful to find out the source of timing system failure and fix it.

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TIMING SYSTEM

Original Timing System

The maximum beam repetition rate is 50Hz limited by the modulators of high-power rf system. A 50 Hz monocycle pulse with a width of 1 ns and the 571.2 MHz clock of about 36 dBm are combined in a trigger transmitter module at the main timing station [4]. The superposition waveform of the 50 Hz timing and the 571.2 MHz clock signals is transmitted through a 30-D coaxial cable as shown in Fig. 1. The output power level is stabilized within 1% by an amplitude gain controller, and the phase is well stabilized within 3 ps (rms) by a phase-locked loop. This signal is divided and distributed to the each of the local timing stations with a low loss and good phase stability. At the each local station, the trigger receiver module decouples this signal into the 571.2 MHz clock and 50 Hz timing signals. The 50 Hz timing signal is finally fed to the modulator of high-power klystron after applying a suitable amount of delay by a delay module.

The timing signals with different amounts of delays are generated at the local timing stations. The timing delay

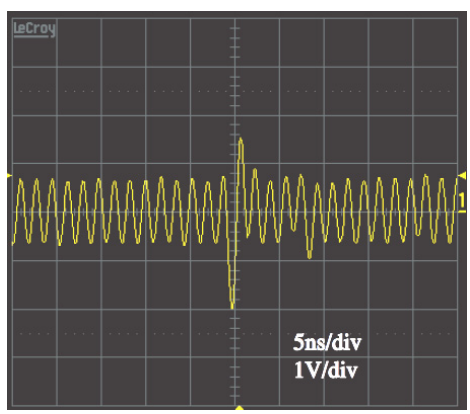

Figure 1: Output waveform of trigger transmitter module. The 50 Hz timing signal is superimposed on 571.2 MHz clock signal.

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modules called TD4V, TD4, and TD4R are based on the VME, CAMAC, and RS232C interfaces, respectively. In these modules, an ECL counter of 16 bit can delay the input signal up to around 114 μs in steps of 1.75 μs, and its timing jitter is about 3 ps (rms). The intended use and the number of modules are summarized in Table 1.

The software for the timing signal control is based on client/server architecture to encapsulate the hardware differences from the client applications. The control command setting the delay on the client side is provided to the each module through the RPC layer. The linac operators can easily change the delay settings to the optimized ones through the command line or graphical user interface (GUI). Though the integrated linac timing system has been stably utilized for the daily beam operation, the timing system upgrade was required for the simultaneous top-up operation.

Event-based Timing System

Table 1: Timing delay modules of original system.

Location	Electron gun	Main timing station/ Sub-booster	Local timing station
Delay module	TD4R	TD4	TD4V
Interface	RS232C	CAMAC	VME
# of modules	1	108	63
Intended use	e- beam timing	High power/sub-booster klystron, Low-level rf, beam monitor timing	High power klystron, SLED timing

The power supply failuers of CAMAC-based system have been occuered several times during the linac beam operation. The replacement work of CAMAC crate interrupts the beam operation for hour or more. Futuermore, the CAMAC-based system is not controllable at the time interval of 20 ms, which is required for the the simultaneous top-up operation. From these resons, the many timing modules have been replaced by a new event-based timing system. We have chosen the series-230 VME-based event system as the new timing system [5, 6]. It has been originally developed for Diamond light. Recently, the many accelerator facilities have already adopted this system. An event generator (EVG) and the event recievers (EVRs) have been installed at the main timing station and local timing stations, respectively. The EVRs can receive the timing information through an optical fiber. EVRs can provide the information as follws:

- Sequence of programmed events in a pulse,
- Regenerated clock signal,
- Up to 14 delayed timing signals,
- Shared data buffer up to 2 k bytes.

The clock signal of 114.24 MHz, which drive the first sub-harmonic buncher of linac, is fed to the EVG as master clock. The EVG output can be transmitted to 20 EVRs through the fanout modules by the multi-mode or single-mode optical fibers. The CPUs and the operating system of the VME computers are MVME5500 and VxWorks-5.5.1, respectively. The combination was chosen to satisfy the realtime performance required for the simultaneous top-up operation. The EPICS driver software is employed for the affinity of linac control system. Since the installation of the EVG and EVRs drastically reduced the number of used TD4/TD4V from 172 to 17, the robustness and maintainability of the timing system have been much improved.

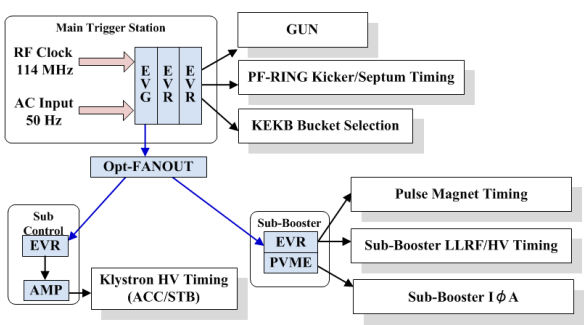

Figure 2: Schematic drawing of event-based timing system and timing signal distribution at the KEK linac.

TIMIMG WATCH DOG SYSTEM

Watchdog Module of 50 Hz Timing Signal

In the KEK linac, the modulators of high power klystron should be triggered by the proper time interval of 20 ms. when the trigger signal interval is longer or shorter than 1 ms with respect to the fiducial timing interval of 20 ms, the modulator turns off for the machine protection. The noise signals could trigger the modulators in the shorter intervals. On the other hand, the longer intervals could be caused by the misfire of the timing module.

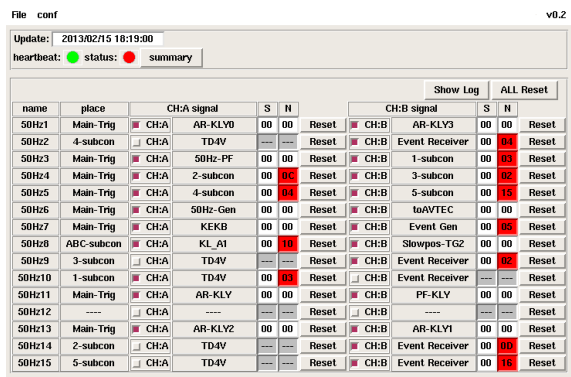

Figure 3: GUI for 50 Hz timing watchdog module.

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For the long-term stable operation, it is indispensable to monitor the timing signal interval and signal loss continuously. For this purpose, the watchdog module of 50 Hz timing signal has been developed and utilized for the linac operation. It is a NIM-based module of one standard width with four LEMO connector ports, and the both NIM and TTL level signals are acceptable inputs. The module has a 100 Mbps Ethernet port by which the control software can send the commands and receive the status information. All failure information of the 50 Hz timing intervals have been accumulated into EPICS and CSS Archivers since the server software is developed as an EPICS framework. When an abnormal timing interval is detected, the linac operators can get immediately the failure information by the GUI panel as shown in Fig. 3. Fifteen watchdog modules in total have been installed at the main timing station and six sub-control rooms. They have been helpful for a quick finding of an abnormal timing interval. Especially, it makes us easy to isolate the problem between the timing modules and the others.

TDC for the Timing Jitter Monitor

Another useful tool is to monitor the accurate timing interval. Figure 4 shows a timing signal chart example for the high power klystron. The trigger signal sequence of 50 Hz is continuously delivered to the high power klystron modulator. Each sequence consists of the timing for the high voltage, rf pulse, SLED timing, and so on. The relative interval between each signal should be constant since the variation of timing interval with respect to reference value affects the beam energy, which causes the deterioration of beam orbit and emittance.

A time-to-digital converter (TDC) could be useful for monitoring the relative interval among the different timing signals. We developed a new TDC module by using Almazillo-9 (Atmark Techno, Inc.), which is a tiny CPU module based on ARM processor [7], and TDC-GP1 (acam-messelectronic gmbh) [8]. Table 2 summarizes the main specification of TDC module. This module has 10 BNC ports as monitor inputs and one port as reference signal input in which the NIM-level signal is acceptable. The measurement time resolutions are 1 ns and 100 ns with the duration of 3.27 ms and 200 ms, respectively. In our case, the measurement mode of 1 ns resolution is interested since the same timing sequence is repeated in the time interval of 20 ms.

The module is running on Linux kernel 2.6.12. The cross platform environment called ATDE, which is

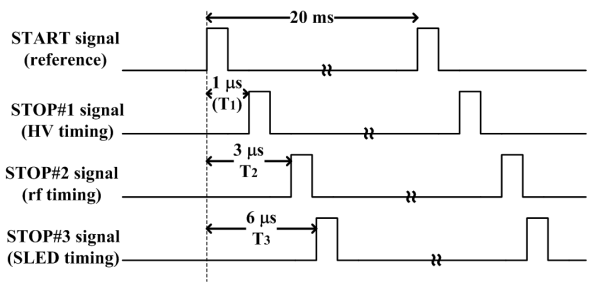

Figure 4: Schematic drawing of timing signal structure for the high power klystron.

Table 2: Specification of TDC module

# of input	10
Input signal	NIM
Measurement duration	3.27 ms (200 ms)
Measurement resolution	1 ns (100 ns)
CPU	ARM920T
CPU/bus clock	200 MHz/100 MHz
Interface	Ethernet
SDRAM	64 MB
FLASH	8 MB

distributed by Atmark Techno, Inc., and VMware were utilized for the software development. An EPICS device support for the TDC module consists of the binary output and waveform type records. The binary output record is used for the control of start and stop for the TDC measurement. We use the waveform record as an array of 50 measurements, each of which includes 14 parameters: the global counter value, timestamp, time interval data from 10 channels, and measurement status (normal/anomalous). The long-term data acquisition will be tested soon after a slight modification is applied to the firmware on Almazillo-9, and its result will be presented elsewhere in the near future.

SUMMARY AND FUTURE PLAN

The timing system is one of most essential part for the KEK linac aiming at the complicated beam handling. The new timing signal watchdog systems are developed and stably utilized for the KEK linac control system. Toward SuperKEKB project, all timing signal will be monitored by the new TDC modules developed here. It is expected to support future SuperKEKB operation with more complicated configurations.

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