OVERVIEW OF THE CSNS/RCS LLRF CONTROL SYSTEM

X. Li#, H. Sun, W. Long, C. L. Zhang, F. C. Zhao
Institute of High Energy Physics, Beijing 100049, China

Abstract

The rapid cycling synchrotron (RCS) RF system of China Spallation Neutron Source (CSNS) is composed of a ferrite loaded RF cavity, a high power tetrode amplifier, a bias supply of 3000A and a digital low level RF (LLRF) control system based on FPGA. The main functions of the LLRF control system are to provide a RF drive signal, to control the frequency, the amplitude and the phase of the accelerating voltage according to the working pattern, to control the amplification process in the amplifiers and the resonant state of the cavities, and to compensate the heavy beam loading. This paper will present the design and structure of the LLRF system, and show preliminary results of performance tests.

INTRODUCTION

China Spallation Neutron Source (CSNS) is composed of an H^- linac and a proton rapid cycling synchrotron (RCS). It is designed to accelerate proton beam pluses to 1.6 GeV, striking a metal target to produce spallation neutron for scientific research. The injection and extraction energy of the beam in CSNS/RCS are 80MeV and 1.6GeV respectively with a repetition rate of 25Hz. The ring RF system is designed to provide the maximum RF voltage of 165kV and operate on the harmonic number h=2. The RF frequency range is from 1.02MHz at injection to 2.44MHz at extraction, as shown in Fig.1. frequency patterns during accelerating time of 20ms.

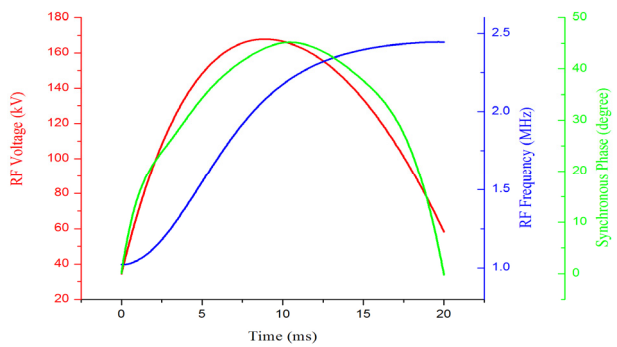

Figure 1: RCS RF voltage, synchronous phase and RF.

The CSNS/RCS LLRF control system is designed for each of eight cavities to achieve required acceleration voltage amplitude and phase regulation of ±1% and ±1deg, respectively. The main functions of the RCS LLRF control system are to provide a RF signal to drive the RF power source. According to the working pattern, the frequency, the amplitude and the phase of the RF signal should be carefully controlled. The LLRF control system should also take care of the resonant state of the ferrite loaded cavity and the high beam loading effect to make sure of the stability of the RF system.

SYSTEM OVERVIEW

Considering system compatibility and bandwidth, CPCI bus is adopted. The hardware platform includes the CPCI6020 CPU, the CSNS standard timing board to receive system clock and event trigger, the custom CPCI carrier to realize all data processing and control arithmetic for control loops. The CPCI hardware is arranged into two CPCI creates. One is for acceleration voltage control and cavity dynamic tuning. Another is for beam orbit correction and beam loading compensation.

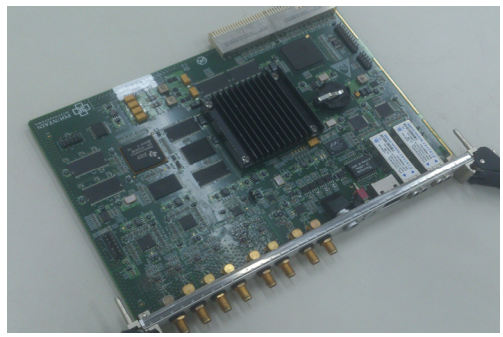

Figure 2: Custom CPCI carrier board.

The custom CPCI carrier is the heart of LLRF control system, shown in Fig.2. It features one Stratix III EP3SL150 FPGA which provides 142.5K equivalent logic elements. It also includes high performance TMS320C6416T DSP, PCI9656 bridge chip, high speed ADC and DAC, optical interface and Ethernet port.

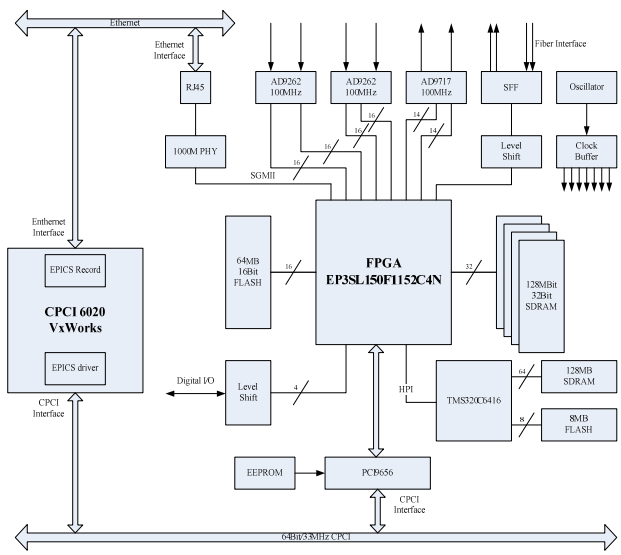

Figure 3: RCS LLRF system configuration.

lixiao@ihep.ac.cn

ISBN 978-3-95450-122-9

Operation command and control data exchange protocol between the CPCI6020 and the CPCI carriers were carefully defined. The custom driver was developed to access specified registers on CPCI carriers from CPCI6020 running the VxWorks operating system. Adhering to the CSNS control standard, the LLRF control system is Experimental Physics and Industrial Control System (EPICS)-based. EPICS drivers have been developed to provide user interface through standard Channel Access protocol. Each custom CPCI carrier has an allocated time slot of 2.25ms for transmission data in 25Hz system operation and the actual bandwidth is greater than 200MB/s. Fig. 3 shows the configuration of the LLRF control system.

CONTROL ARCHITECTURE

Each cavity of the CSNS/RCS RF system has independent LLRF control system based on FPGA which is composed of 7 control loops including cavity voltage loop, synchronous phase loop, cavity tune loop, tetrode grid tune loop, beam loading compensation loop, orbit feedback loop, and direct RF feedback loop.Fig.4 shows the block diagram of the LLRF control system.

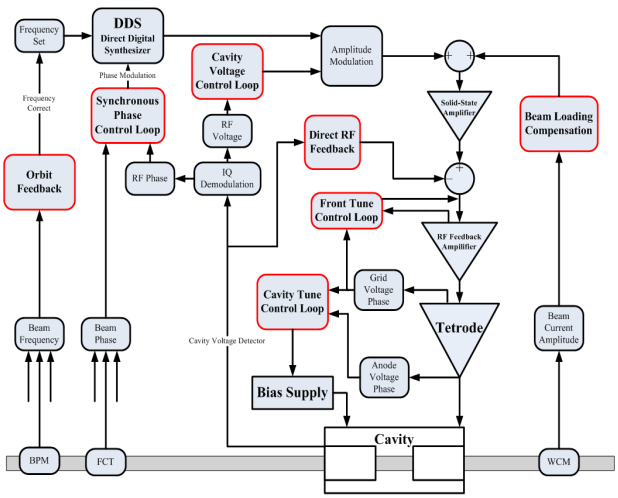

Figure 4: block diagram of the LLRF control system.

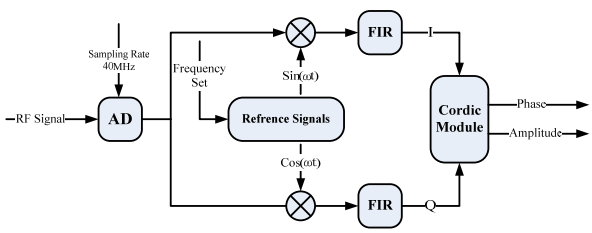

Figure 5: Procedure of signal processing.

For most control loops in CSNS/RCS LLRF control system, the procedure of signal processing works in much the same way. The master oscillator and reference signal are both generated by DDS (Direct Digital Synthesizer) module. All RF signals are sampled with 40MHz, and then digital signals are separately multiplied by two reference signals for orthogonal demodulation. A 70 taps FIR low-pass filter is adopted with 1.75μs delay. The Coordinate Rotation Digital Computer (CODIC) algorithm is also used to compute trigonometric function and get the amplitude and phase of the signals. Fig.5 shows the procedure of signal processing.

Cavity Voltage Loop

The cavity voltage loop exists individually for each cavity at (h=2), and makes the cavity voltage follow a pattern shown in Fig.1. Each cavity has two acceleration gaps in parallel. For one gap, the minimum voltage is 1.3kV and the maximum voltage is 10.3kV.

There is a feedforward compensation option to decrease the following error induced by the rapid change of cavity voltage. The feedforward compensation mainly includes two parts, one is average of the amplitude modulation values of the past few cycles, and the other is the amplitude error multiplied by a certain factor.

Synchronous Phase Loop

The synchronous phase loop controls the phase between the accelerating voltage of each cavity and the longitudinal beam signals monitored with Fast Current Transformer (FCT).

Cavity Tune Loop

The cavity tune loop is fed by the phase between grid voltage of tetrode and the cavity voltage. The change of resonant frequency of the cavity from 1.22MHz to 2.44MHz corresponds to the bias current changing from about 300A to 2900A.

Due to the bandwidth limitation of bias supply, a feedforward compensation is adopted for the 25Hz system operation. The algorithm is similar to cavity voltage loop. The actual bias current of the past few cycles and the tuning error are used to generate a feedforward table.

Tetrode Grid Tune Loop

The tetrode grid tune loop is used to compensate the parasitic capacitance of the tetrode grid, and ensure system gain and stability in operating frequency range. a linear bias supply of 10A is used to change the inductance of a ferrite-loaded low-Q resonant circuit. There is only a feedback loop for the tetrode grid tuning. Except for this, both of the tetrode grid tune loop and the cavity tune loop have the same operating principle.

Beam Loading Compensation Loop

The circulating current in CSNS/RCS is fairly high, and the beam loading effect must be carefully considered. A classic feedforward algorithm is adopted for the beam loading compensation. The beam signal is picked up by Wall Current Monitor (WCM), and added into the RF drive signal with an opposite phase. The fundamental component of the beam signal is taken out, and given the proper gain and phase.

Because of two stage of tuning loops, some phase error

will be introduced. An adaptive algorithm is now being developed for adjusting the phase setting of the feedforward algorithm.

Orbit Feedback Loop

The orbit feedback loop is reserved to adjust the initial frequency setting. The beam signal is picked up by Beam Position Monitor (BPM), and used to compute the modification value.

Direct RF Feedback Loop

The RF feedback loop is adopted to reduce transient beam loading and enhance the dynamic performance of the RF system. A small fraction of cavity voltage is picked up and fed back to the feedback amplifier. The feedback gain is about 20db, and the phase shift in the feedback path is guaranteed by the two stage of tuning loops.

RF SYSTEM TEST RESULTS

The high power integration test was completed on the prototype of RF system, with the cavity voltage loop, cavity tuning loop, tetrode grid tuning loop, and RF feedback loop closed. A schematic diagram of the test is shown in Fig.6. The maximum cavity gap voltage can reach to more than 10kV during 20ms, RF frequency sweeping range of 1.022 ~ 2.44MHz.

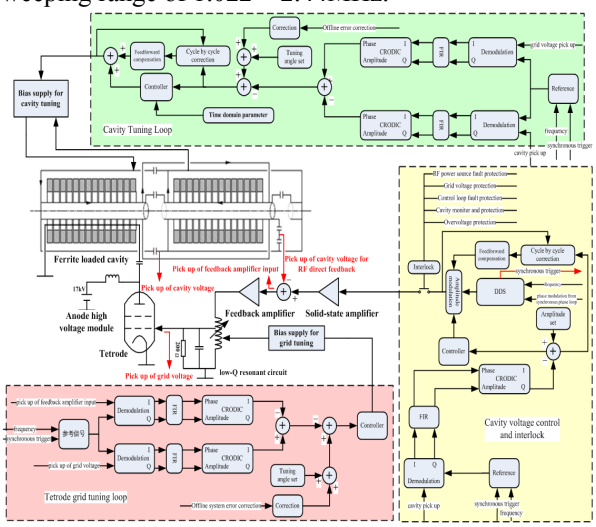

Figure 6: Schematic diagram of the high power test.

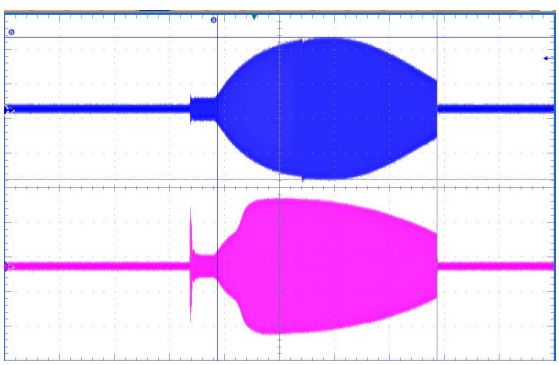

Figure 7: Cavity voltage (blue) and grid voltage (purple).

Fig.7 shows the RF cavity voltage waveform. An undesired resonance with higher order harmonic component of 7MHz had been observed on the cavity voltage (Fig.7). It is caused by the distributed inductance of links and cavity gap capacitors. In the new cavity design, the shape of gap links from circular coaxial to rectangular coaxial is improved to reduce its distributed inductance and economize the space.

The RF voltage error was less than ±1% with the feedforward compensation (Fig.8), and RF system detuning angle within ±5 degree except the beginning of sweeping with a lager detuning angle of <±10º (Fig.9).

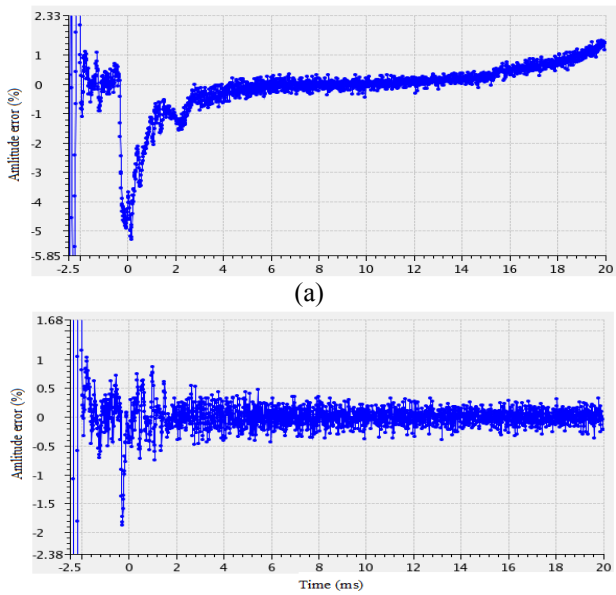

Figure 8: Cavity voltage error in one cycle without (a) and with (b) feedforward compensation.

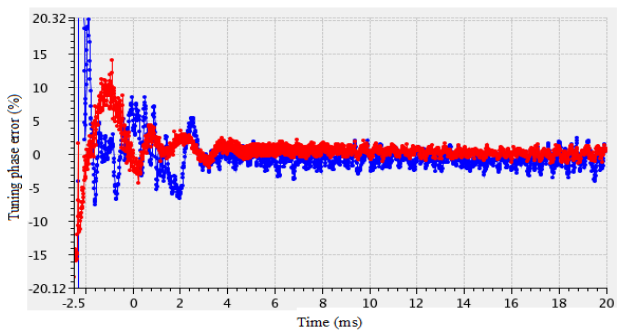

Figure 9: Cavity tuning error (blue) and grid tuning error (red) in one cycle (20ms).

REFERENCES

[1] Wei Tao, Fu Shinian, Qin Qing, et al. RF trapping and acceleration in CSNS/RCS[J]. *Chinese Physics C*, 2008, **32**(6): 437-441.

[2] D. Boussard, et al. Control of cavities with high beam loading[J]. *Nuclear Instruments and Methods in Physics Research (Section A)*, 1985, **32**(5): 1852-1856.

[3] H. Sun, et al. RF system of the CSNS Synchrotron[C]. In this conference.

[4] Robinson. K W. Stability of beam in radiofrequency system[R]. CEAL-1010, 1964.

ISBN 978-3-95450-122-9