DEVELOPMENT STATUS OF SINAP TIMING SYSTEM

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Abstract

After successful implementation of SINAP timing system in PLS-II project in 2011, SINAP v2 timing system development was started. The bidirectional data transfer and EVG cascaded function are supported in v2 system. The hardware structure is also modified, where a new product, called VME-EVO, could be configured as EVG, FANOUT or EVR. Besides VME modules, PLC-EVR is developed as well, which complies with Yokogawa F3RP61 series. Based on upgraded hardware architecture, the jitter performance of SINAP v2 timing system is improved remarkably.

INTRODUCTION

We started to develop SINAP timing system since 2007. The prototype of SINAP v1 timing system was completed and tested at LINAC of SSRF in January 2010. PLS-II project introduced v1 system, and first beam accumulation in storage ring was realized in August 2011 [1][2]. Subsequently, SINAP v2 timing system started to design. And we will implement v2 system for different projects.

SYSTEM DESIGN

Thanks to rapid development of high-speed serial communication and FPGA technology, the event timing system became the sophisticated solution in the large-scale accelerator facilities, especially for the 3rd generation light source. The main advantage of event timing system is that triggers and clocks could be transmitted in the same fiber-optic network. This means wherever the timing system fiber network reaches, triggers and clocks could be provided.

SINAP v1 Timing System

In SINAP v1 timing system, the range of event clock is from 120MHz to 135MHz. EVG (event generator), EVR (event receiver) and FANOUT are standard 6U VME modules. The delay adjusting step of TTL outputs is one event clock period, and the adjust step of SFP output in EVR front panel could reach to 1/20 event clock period and 5ps. The v1 system structure is illustrated in Fig. 1.

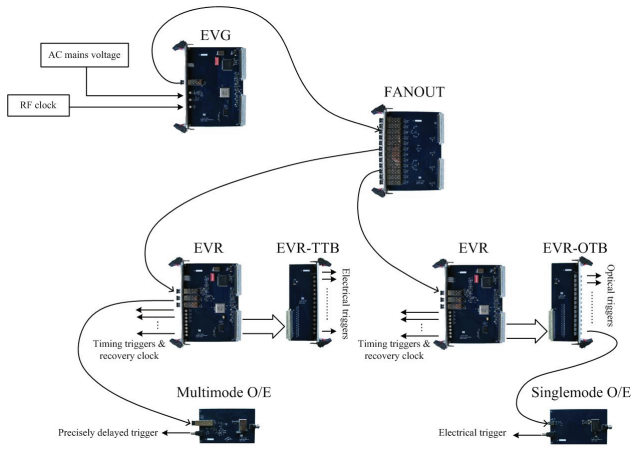

Figure 1: Structure of SINAP v1 timing system.

SINAP v2 Timing System

In SINAP v2 timing system, deterministic data transfer and event distribution could be satisfied in the same fibre networks[3]. The range of Event clock is from 60MHz to 135MHz. EVG cascading function is supported, so different event clock could be allowed in the same event timing system. The delay step of all outputs could be one event clock period, 1/20 event clock and 5ps.

The system structure is illustrated in Fig. 2. Because introducing the new VME-EVO modules, types of hardware modules are simplified. VME-EVO could be configured as EVG, FANOUT or EVR by software. VME-EVE could only be used as EVR. If VME-EVO is configured as EVR, its fibre outputs could be demodulated by STD-OE module, which could be used inside high power device.

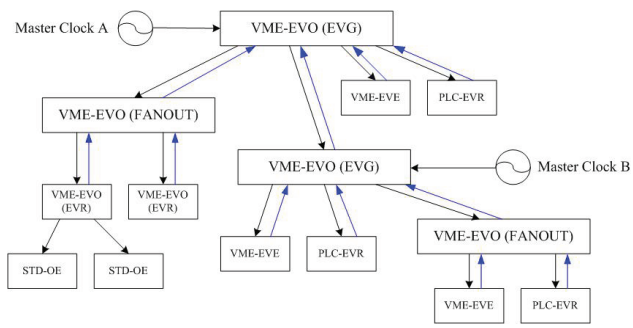

Figure 2: Structure of SINAP v2 timing system.

STD-OE module is the standard 19inches 1U stand-alone module, which contains four independent channels.

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PLC-EVR module was developed in v2 system, which complies with Yokogawa F3RP61 series. The module is one-slot width, and requires external 5V/3A DC power supply. Heat dissipation was considered to maintain the module stability in no-fan and sealed environment. I/O register addressing mode and interrupt function are supported.

The four modules mentioned above are illustrated in Fig. 3.

Figure 3: Hardware of SINAP v2 timing system.

TEST RESULTS

We use Tektronix TDS8000B oscilloscope and 80E03 Sampling Module to measure the short-term jitter between output trigger from EVR and RF reference clock. As shown in Fig. 4, the RMS jitter is about 10.1ps. The measurement background RMS jitter in shot term is about 1.5ps.

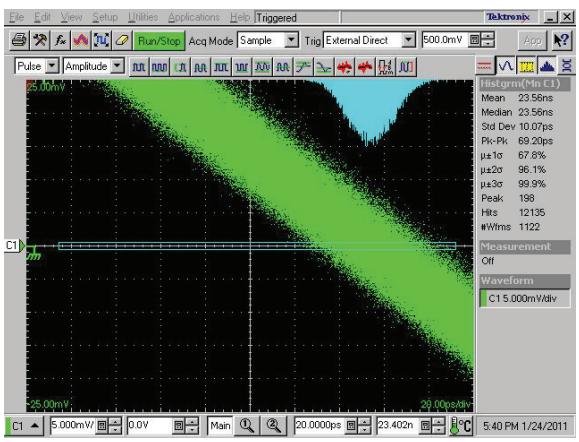

Figure 4: Jitter of SINAP v1 timing system.

For SINAP v2 timing system, we use the same test bench to measure the short-term jitter of output trigger from VME-EVE and RF reference clock. As shown in Fig. 5, the RMS jitter is about 6.3ps. The jitter performance of PLC-EVR is similar with VME-EVE. We measured the long-term jitter for 20 hours as well, which is about 8.3ps and illustrated in Fig. 6.

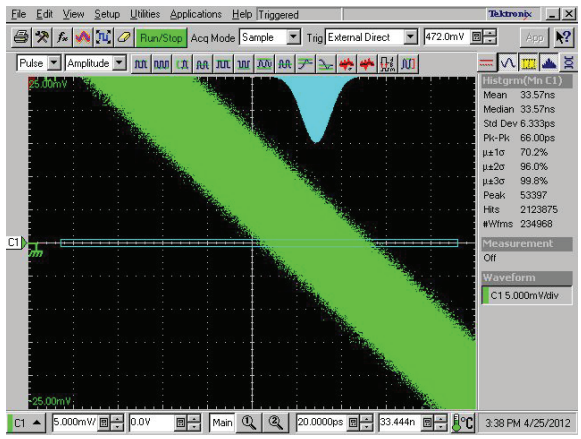

Figure 5: Jitter of SINAP v2 timing system.

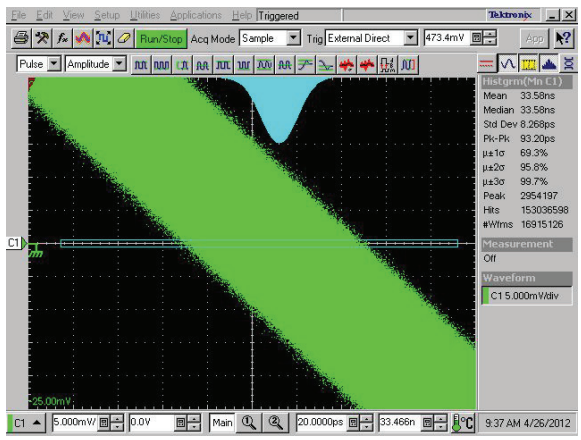

Figure 6: Jitter of SINAP v2 timing system with long-term drift.

CONCLUSION

As shown above, performance of SINAP v2 timing system improved remarkably compared with v1 system. After successful implementation at PLS-II project, SINAP timing system attracts the attention of many projects under construction or newly approved. We collected and considered different requirements, and then designed the structure and hardware of v2 system[3]. So, SINAP v2 timing system could satisfy requirements of timing system in different accelerator facilities.

With experience in hardware design of SINAP timing system, the jitter performance within several picoseconds was realized. In future, we will focus on fibre laser system to achieve sub-picoseconds jitter performance for

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higher requirement, which is our outline plan in SINAP v3 timing system development.

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