THE DEVELOPMENT OF LLRF SYSTEM AT PAL*

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Abstract

The PAL has been developing the low level radio frequency (LLRF) system. The required field stabilities of the LLRF system are within ±0.75 % in amplitude and 0.35° in phase in a cavity. All the hardware including RF front–end, FPGA with peripherals such as ADC, DAC, clock generator and digital interface were assembled. The sub-modules for the RF signal processing were written by VHDL and integrated to test at the local facility. The Microblaze software processor was implemented to make the system simple in interfacing to peripherals and to secure flexibility later.

This paper described the Microblaze processor which was ported into the Vertex6 FPGA. The test results of the analogue RF front-end and the experimental results of the each VHDL module like filter, CORDIC, IQ demodulation etc. were showed.

INTRODUCTION

With the development of the high performance integrated circuits such as the high throughput analogue to digital converter, the field programmable gate array (FPGA) etc., the digital technologies are begun on application for the accelerator systems.

The PLS-II parameters related to RF systems are listed in the table 1. The superconducting RF cavities were installed in the storage ring and have been operating since August 2012.

Table 1: RF Relative Parameters of the PLS-II

Parameters	Unit	PLS-II
Energy	GeV	3.0
Current	mA	400
Emittance	nmrad	5.9
RF frequency	MHz	499.973

Many accelerator laboratories over the world adopted the digital low level radio frequency (LLRF) systems that gave the satisfied stabilities to accelerator operation [1, 2]. The LLRF system was implemented using the Vertex6 FPGA (XC6VLX75T) as a main controller. The FPGA board worked as a mother board. The two ADC boards, one DAC board and one clock generator are assembled on the FPGA board.

The RF analogue front parts like a RF transmitter for 500 MHz output, a local oscillator (LO) of 450 MHz and four 500 MHz RF inputs are assembled and tested. The test results of the analogue front-end are shown. The VHDL modules to calculate the RF field control were written and tested. The Microblaze processor for building an embedded system was described. The some test results of the cascaded integrator comb (CIC) filters, I & Q modulation and demodulation, and CORDIC were shown in this paper.

LLRF SYSTEM

RF Front-End

RF front-end divided into three parts as a RF transmitter, a LO circuits and four RF receivers. The intermediate frequency (IF) of 50 MHz which was controlled by the vector sum of I & Q components using a DAC was up converted to 500 MHz by the double balanced mixer ADE-10 from Minicircuits. The IF was passed to the LPF of 60 MHz bandwidth filter to reduce the small distorted signal components. The band pass filter of a SMBP-500 from RLC electronics was connected after mixer to remove the unnecessary harmonic components. And this signal was amplified to have certain required power. The LO was generated similar to RF transmitter but the filter has 450 MHz center frequency. The 500 MHz transmitter and the LO are assembled in a PCB as shown in the Figure 1.

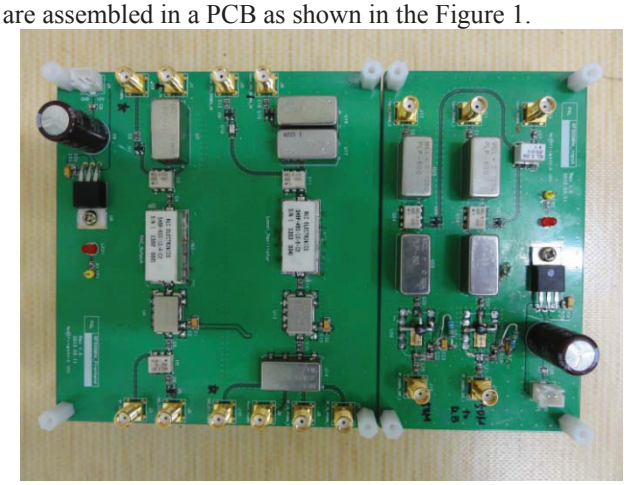

Figure 1: RF front-end PCBs. A LO of 450 MHz, a 500 MHz transmitter and two RF receivers in sequence from left to right.

The RF signal of 500 MHz incoming from the cavity was filtered by a low pass filter to remove the higher

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noise components. This signal was converted down to the IF by the mixer ADE-10H from Minicircuits. The mixer has a good L-R isolation of 39 dB, a high IP3 of 30 dBm and a low power level of 17 dBm for the LO. The mixer output signal was filtered by a low pass filter again to get the only IF signal and then amplified by the MAV-11. The two RF receivers are assembled in a PCB. When powers of both RF cavity input and the LO are inputted with 9 dBm, the output signal of the IF was shown in the Figure 2.

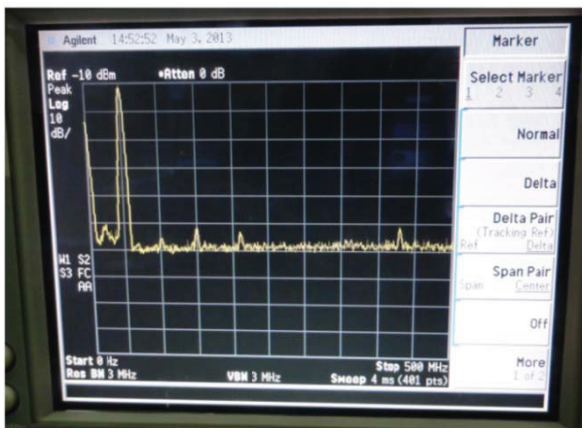

Figure 2: The IF output signal down converted from the 500 MHz RF input.

IQ Demodulation and CIC Filter

The LLRF system uses digital signal processing techniques, which are based on IQ signals to regulate the RF field signals like the Figure 3. So first, the LLRF system converts the 50 MHz analogue signals from RF front end to digital signals with the ADC sampling clock of 40 MHz. The 40 MHz sampling frequency is a 4/5 times of the IF signals and it satisfied the condition of IQ sampling method. Therefore, the sampled data from ADC has repeating pattern of IQ signals. The data stream is subsequently separated into IQ signals, respectively by a IQ demodulator within the FPGA board as shown in figure 4[3]. The IQ signals provide information of RF field signal by the simple mathematical equation and have symmetrical characteristic each other, so that it is suitable to utilize the digital signal processing.

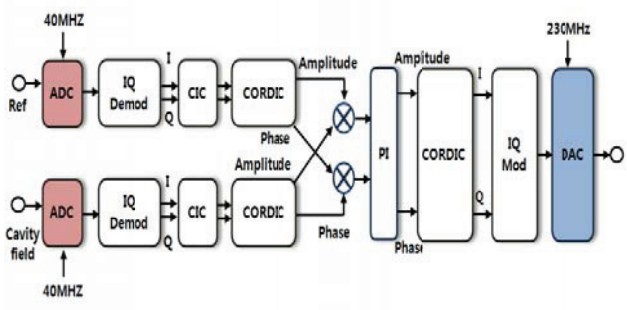

Figure 3: Signal-processing algorithm for amplitude and phase control.

The jitter in ADC sampling clock makes the IQ signals to have ripple components. In order to remove them, the LLRF system adopts the CIC filter among digital filters to take into account the influences between stability and latency. The CIC filter needs small tap number to get the useful output responses comparing to other digital filter such like FIR. The LLRF system uses the 3-tap CIC filter to filter out the high frequency components and Figure 5 shows the test result of the filter. The amplitude of I term was reduced to about -6 dB after filter processing.

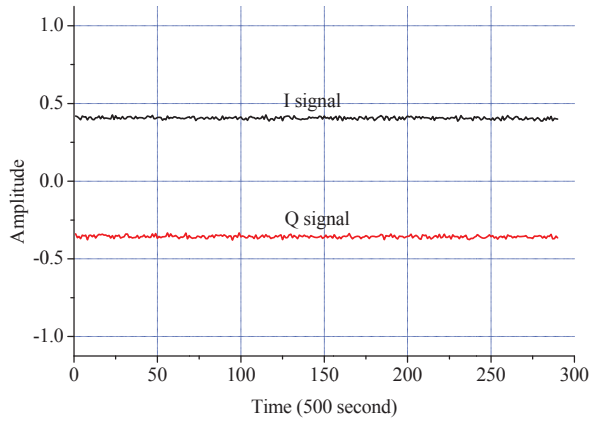

Figure 4: Measurement data of IQ demodulation test.

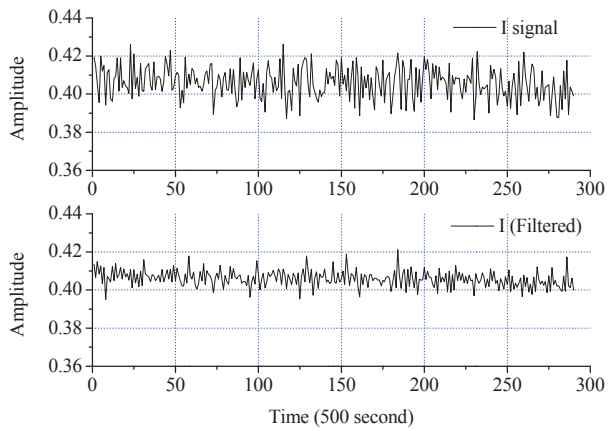

Figure 5: Measurement data of CIC filter test.

CORDIC and PI Control

In order to calculate the amplitude and phase of RF field from IQ signals and vice versa, The LLRF system adopts the CORDIC method. It can calculate the trigonometric functions without multiplication process. Thus, it spends small resources in a FPGA and takes short time for program running. In this LLRF system, 12-tap CORDIC is adopted and it uses three clock periods for calculation of the amplitude and phase. The Figure 6 shows the tested result of CORDIC and its maximum error was 0.0895 % in terms of amplitude and phase [4].

The outputs of CORDIC are compared with reference value and then the errors are fed into PI controller. The PI controller makes the steady state error to zero related with amplitude and phase of the RF field. Therefore, the LLRF system can provide stable RF signal to RF high power system. The propagation delay at the hardware and signal processing should be small to be able to make P-gain high. That made the system stability better.

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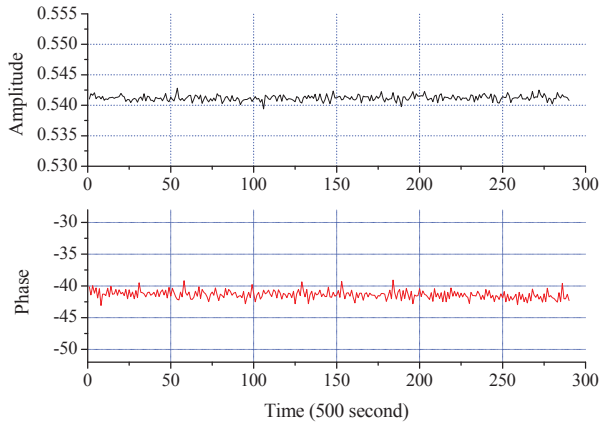

Figure 6: Amplitude and phase responses which are calculated by the CORDIC algorithm.

IQ Modulation

The LLRF system modulates the controlled IQ signals using lookup tables and a DAC with 230 MHz sampling clock synchronized with the ADC sampling clock. The test results with a lower DAC clock at 160 MHz showed a poor frequency responses, thus the higher clock of 230 MHz was accepted to the system. The translation of IQ signal to the IF signal takes place in digital board and the LLRF system is not sensitive related with gain imbalance and skew component[5]. However, the 230 MHz DAC clock is not enough high to generate the 50 MHz IF signal with small distorted signal. Thus, the LLRF system utilizes the band pass filter with narrow bandwidth in the RF transmitter board.

Microblaze Processor

The Microblaze software processor was installed in the LLRF logic to make the interface logic simple. The Xilinx Platform Studio has many IPs such as CAN, Ethernet, FIFO, USB, DMA, Memory controller etc. [6]. The LLRF system included three UARTs, one timer, one interrupt controller and GPIO interface as the Figure 7.

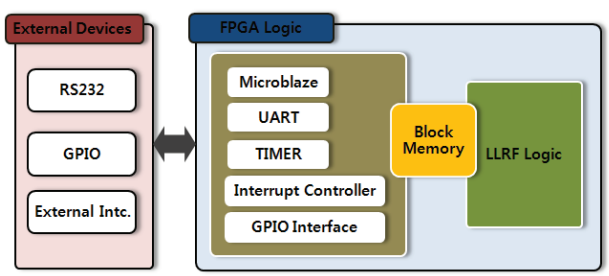

Figure 7: Conceptual block diagram of Microblaze micro processor for the LLRF.

The Microblaze has four memory blocks of 1024*32 for data exchange with the user LLRF logic. The memory interface control clocks such as chip selector signal, read and write signals were generated by the internal VHDL logic.

All the control signals like set phase, amplitude, P & I gains for PI compensator etc. and monitoring signals such as cavity amplitude, phase, forward power etc. are transferred in both ways by these memory blocks. The figure 7 showed a conceptual block diagram how to use the block memory between the Microblaze and the LLRF user logic. The Figure 8 showed the some parameters at the console, which were provided by the Microblaze through the RS232C.

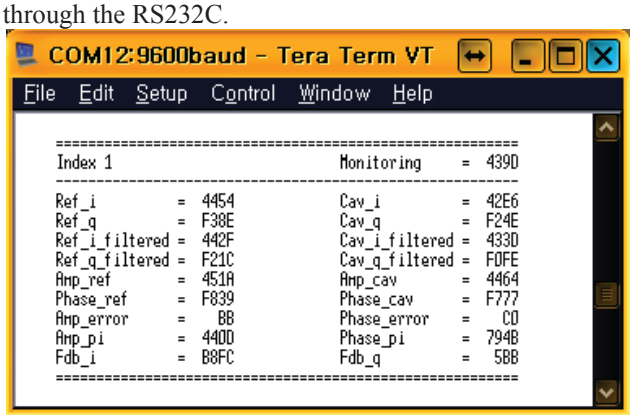

Figure 8: Parameters provided by the Microblaze.

CONCLUSION

A digital controlled LLRF system has been developing for PLS-II RF system. The Vertex6 FPGA was worked as the main controller with some peripherals like ADCs, DAC, clock generator, and so on. RF front-end parts such as RF receiver, RF transmitter and LO, were assembled and tested. The RF receiver showed good the signal to noise ratio about 50 dB to the frequency responses. The both LO and 500 MHz transmitter also showed a signal-to-noise ratio. The Microblaze processor was also included into the LLRF VHDL logic and it gave the VHDL logic simple. The communication between a consol and VHDL logic through the Microblaze was worked well. The VHDL modules including I&Q modulation and demodulation, CORDIC, CIC filter etc. are simulated and integrated into the LLRF processor. The output responses of the IQ demodulator showed good responses. The CIC filter reduced the input noise about -6dB. The CORDIC module with 12-taps implemented into VHDL logic also showed good responses with error of 0.0895 %.

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