DESIGN AND CONSTRUCTION OF A REMOTE CONTROL FOR THE CADS DIGITAL POWER SUPPLIES*

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Abstract

A remote controlled power supply system includes a data processing system and control at least 76 power supplies, which is designed for the China Accelerator Driven Subcritical system (C-ADS) power supplies system. The system Construction in the mode of integrated control with 1U chassis board, and the hardware parts control core based on Field Programmable Gate Array (FPGA). The software part adopts Experimental Physics and Industrial Control System (EPICS) platform with database and TCP/IP protocol, the administrators can acquire the working parameter through a remote control equipment and control the power supply at the remote site.

INTRODUCTION

Accelerator driven sub-critical system (ADS) is a kind of high efficient nuclear waste transmutation machine (or incinerator), which is the key technique to solve the nuclear waste problem [1]. In the system, the stable and reliable operation of the accelerator magnet power supplies is crucial.

The accelerator magnet power supplies of the ADS can be classified into two types by working mode: the Medium Energy Beam Transport (MEBT), the Cryogenic Magnet (CM), and so on. These accelerator magnet power supplies are almost DC sources.

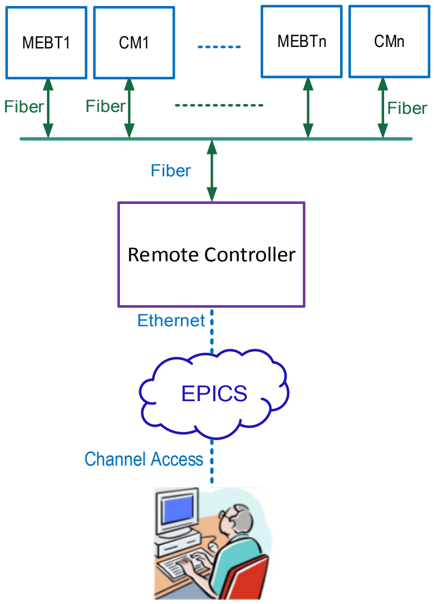

Figure 1: Remote control system design Scheme.

The remote control system includes a signal processing unit and a communication unit. The signal processing unit receives a working parameter of the power supplies and outputs ON/OFF signal to drive the data processing system to output the power ON/OFF signal to switch the state of the power supply state. The communication unit is linked the signal process unit to receive the working parameter and output the working parameter to a communication network with TCP/IP. The administrators can acquire the working parameter through a remote control equipment and control the power supplies at the remote site [2]. The magnet power supply remote control system design scheme is shown in Fig. 1.

SYSTEM DESIGN

Remote control system needs Ethernet devices for the large number of power supplies. We have developed the hardware and software of the remote control system. The hardware consists of two module set–a front signal receiver module and a signal processing module based on FPGA. The software development work is that designing different kinds of EPICS IOC, real-time database, and friendly OPI coincided with the type of power supplies. Fig. 1 shows a block diagram of remote control system.

Hardware System Design

The main function of remote control system is that individual digital commands can be sent from the remote controller to the Power Supply Interface (PSI). After receiving the command, the PSI sets the appropriate power supply command bits, and responds to the remote controller with an echo and the power supply's status. Figure 2 shows the block diagram of a remote controller's hardware.

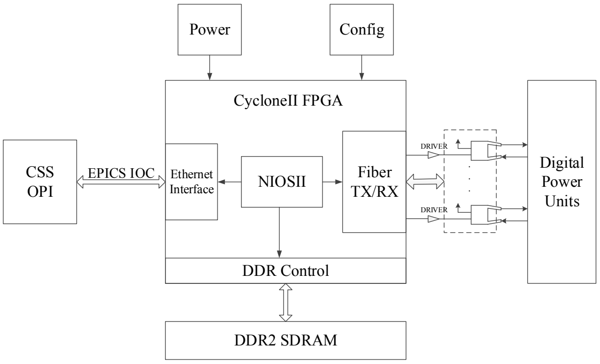

Figure 2: Block diagram of remote controller's hardware.

It consists of four major sections: The Ethernet interface, the fiber TX/RX interface, the FPGA block, and the power module. The ensuing paragraphs give details of

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each section, and the picture of remote controller of power supplies shown in Fig. 3.

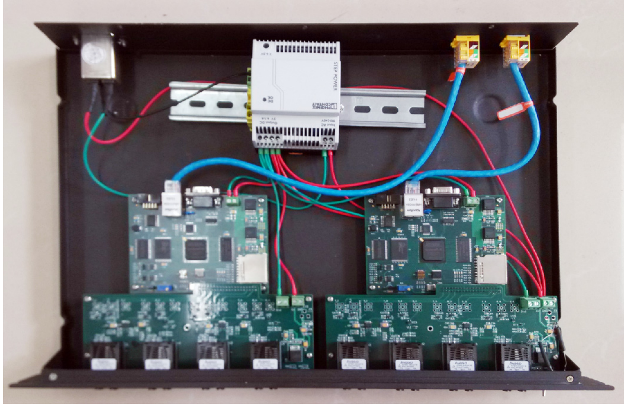


Figure 3: Picture of remote controller of power supply.

The main logic cell of hardware is Altera's FPGA, running with NiosII system. A low voltage fiber optic transceiver (1300nm wavelength, 62.5/125 multimode fiber, AFBR-5803) is used to communicate with a remote controller [3].

There are two fiber optic connections between a remote controller and a PSI; one for the remote controller to transmit set-points and commands to the PSI, and one for the remote controller to receive read-backs and status from the PSI.

Digital Signal Processing

The data is formatted using a self-clocking bi-phase mark encoding, resulting in a data stream running at 5Mbps. This is shown in Figure 4. The carrier is continuous. During idle periods, when no data is being sent, only 'ones' are transmitted.

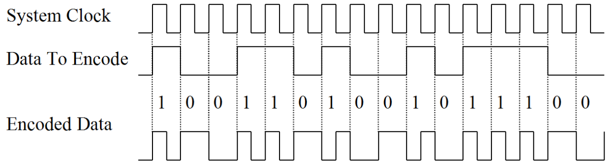


Figure 4: Bi-phase Mark Encoding.

The encoding and decoding functions are performed in the Altera FPGA. The encoder provides a bi-phase mark format. Bi-phase mark has two advantages over standard NRZL data transmission. First, there is always at least one level transition every bit period. This feature makes it easier to synchronize to the signal for decoding purposes. Second, it allows for more stable transmitting power.

Data words sent between a remote controller and the PSI (set-points, read-backs, commands and statuses) are all formatted into a structure called a frame. A frame consists of 43 bits, as shown below in Table.1.

Table 1: Frame Structure

Start(1)	ID(8)	Data(16)	Auxiliary(8)	CRC(8)	Stop(2)

All communications between the remote controller and PSI are initiated by the FPGA. The remote controller initiates the cycle by sending a data stream (set-point, command, status …) to the PSI. And the Sender module load the data, furthermore check data with bit CRC. Once the CRC check is OK, encoding the bit data to a frame (43bits) with bi-phase mark (BMC), then send the frame to PSI and wait reply [4].

Upon receiving this frame, the Receiver module starts data and clock recovery operation. Once the recovery is done, check data with bit CRC again. If the CRC check is OK, the FPGA will receive three frames which are sent from the PSI: status, current and setpoints. The entire communication cycle (from the beginning of the FPGA setpoint frame to the end of the PSI's response frame) take less than 10us. This means that the FPGA can send set-points to the PSI at a maximum rate of 100,000 set-points per second. A flow chart of control code is showed in Fig. 5.

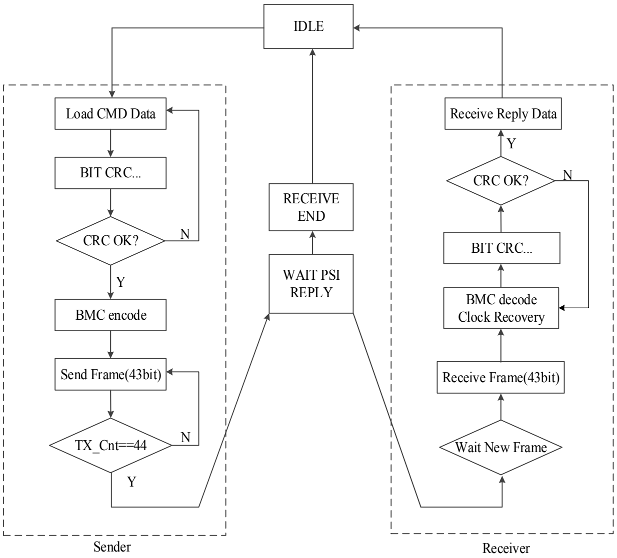


Figure 5: Flow chart of frame sender and receiver.

Software

The software part adopts EPICS platform with IOC database and TCP/IP protocol. EPICS driver is intended to connect an FPGA via TCP/IP to an EPICS IOC, using the so called "send/receive" protocol. However, it can be used for any device sending and receiving blocks of process variables (PVs) in the same way. I highly recommend to connect to the FPGA on a separate physical network using a second network interface to avoid connection problems [5].

The driver and the FPGA periodically exchange data (process variables) over Ethernet. For each direction (IOC to FPGA and FPGA to IOC), there is one fixed size data block that bundles all process variables for this direction. The process variables are identified by their bytes offset in the data block [6].

When the IOC starts, the driver tries to connect to the FPGA which must run a TCP server. If connection cannot be established (e.g. because the FPGA is off) the driver periodically retries to set up the connection. Once connected, the driver waits for data blocks sent by the

FPGA. The FPGA must be set up to send its data periodically. If the driver does not receive any data within a configurable timeout (which should be 2 to 10 times the send period of the FPGA) or the data block does not have the correct size, the driver considers the communication broken and closes the connection. After a short time it tries to reconnect. A flow chart of EPICS driver is showed in Fig. 6.

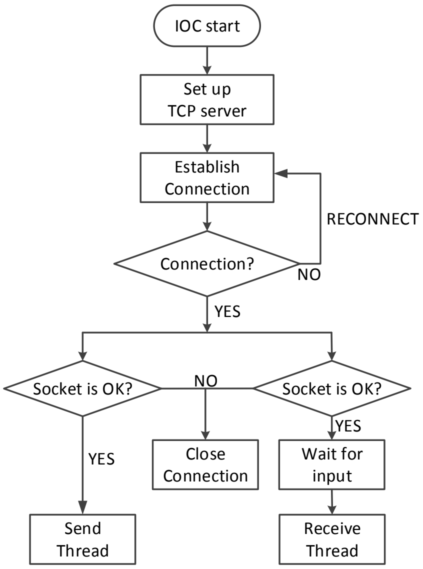
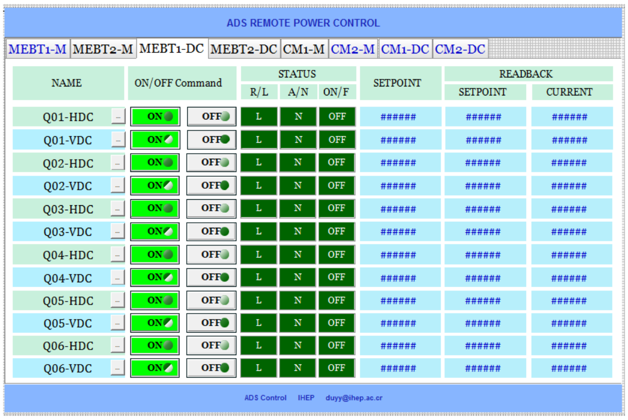


Figure 6: A flow chart of EPICS driver.

The development of OPIs is adopted CSS which jointly developed by DESY, SNS and so on. By now, many libraries in the world begin to use CSS and customize CSS to match their own requirements in order to replace the traditional tools like EDM, Strip Tool, Channel Archive and so on. The OPIs developed by CSS are more beautiful and flexible and can be used for complex control owe to rich tools and plugins are integrated in CSS.

As shown in Fig. 7, operator can turn on or turn off the remote power supplies, and it can display the power status (remote control mode or local control mode, power working state, alarm or normal). In the other hand, it can set-point and read back current easy. And the setting current values OPI as shown below in Fig. 8.


ADS REMOTE POWER CONTROL

MEBT1-M MEBT2-M MEBT1-DC MEBT2-DC CM1-M CM2-M CM1-DC CM2-DC

NAME	ON/OFF Command		STATUS			SETPOINT	READBACK	
			R/L	A/N	ON/F		SETPOINT	CURRENT
Q01-HDC	ON	OFF	L	N	OFF	######	######	######
Q01-VDC	ON	OFF	L	N	OFF	######	######	######
Q02-HDC	ON	OFF	L	N	OFF	######	######	######
Q02-VDC	ON	OFF	L	N	OFF	######	######	######
Q03-HDC	ON	OFF	L	N	OFF	######	######	######
Q03-VDC	ON	OFF	L	N	OFF	######	######	######
Q04-HDC	ON	OFF	L	N	OFF	######	######	######
Q04-VDC	ON	OFF	L	N	OFF	######	######	######
Q05-HDC	ON	OFF	L	N	OFF	######	######	######
Q05-VDC	ON	OFF	L	N	OFF	######	######	######
Q06-HDC	ON	OFF	L	N	OFF	######	######	######
Q06-VDC	ON	OFF	L	N	OFF	######	######	######

ADS Control IHEP duyy@ihep.ac.cr

Figure 7: ADS power supplies remote control OPI.

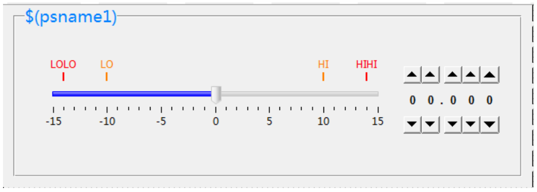


Figure 8: The setting current values OPI.

CONCLUSIONS

This paper presents a novel remote control technique of the accelerator magnet power supplies. After 2 weeks test in labs, every basic function and soft interlock has been implemented, without any mistake. The results show that the output current of DC-DC converter is increased with the increase of control current. The proposed system has presented good performance and capability for remote power control of the accelerator magnet power supplies. The illustrated technique is also capable of remotely monitoring the system performance of the accelerator magnet power control via the Internet from a dispatch center.

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