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A HIGH-PERFORMANCE DIGITAL CONTROLLER BASED ON ETHERNET INTERFACE FOR ACCELERATOR POWER SUPPLY

R. Li, S.Q. Tan, R.N Xu, W.F. Wu,
Shanghai Institute of Applied Physics, P.O.Box 800-204, Shanghai 201800, P.R. China

Abstract

Accelerator applications need extremely precise and highly digitized power supplies for various magnets. A new digital controller for accelerator power supply was developed and implemented. It is a high-performance and multifunctional digital controller with dual-processor system and Ethernet interface. Due to the high resolution Analog to Digital Converter, high resolution Pulse-Width Modulation generator and precise timing design, it can precisely control the accelerator power supply output static or dynamic output. In addition, it also performed well on multi-controller's synchronous control.

INTRODUCTION

The digital controller is consisted of one control card and one Analog to Digital Converter (ADC) card; they are connected by high-speed Serial Peripheral Interface (SPI) through the backboard.

The control card is responsible for communicating and dealing with control operation; the ADC card is responsible for sampling the feedback signals.

The FPGA (Altera Cyclone IV EP4CE40) is embedded with 32-bit hardware floating point multiplier and dual-processor system of Nios II soft core processor. Compare to other single-processor or dual-processor system of the digital controller [1]-[2], the main characteristics of this digital controller are as follows:

- Embedded hardware floating point multiplier and multi-processor system.
- High speed and high stability Ethernet communication.
- Compatible RS232 and Manchester Code communication through optical fiber.
- High resolution PWM output.
- Advanced PID algorithm.
- High resolution ADC.
- High-performance multi-controller's synchronous control.
- Programmable waveform storage and control.

The block diagram of the control card is shown in Figure 1, two pieces flash were used to store the information and waveform data; two RAMs were used for processors; 16 isolated digital inputs and 8 isolated outputs were used for interlock. Ethernet were used as remote control interface; optical fiber was used as trigger input.

The ADC card has a same FPGA with control card and some peripheral components, with a single processor system of Nios II in it, which has a 18bit channel for current and four 16bit channels for voltage.

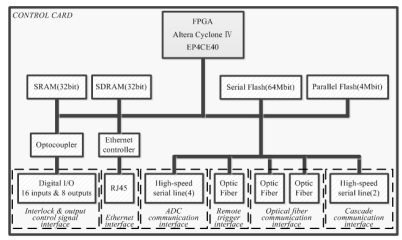

Figure 1: Block diagram of the control card.

DUAL-PROCESSOR OF NIOS II

The two isolated Nios II fast processors which run independently on two different AVALON bus. Each of the processor is integrated with the 32-bit floating-point hardware multiplier which greatly improves the speed of floating-point calculation, and they share data through a dual-port on-chip RAM. The hierarchical Nios II dual-processor system block diagram is shown in Figure 2.

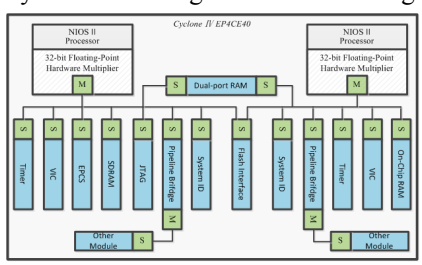

Figure 2: Hierarchical Nios II dual-processor system block diagram.

Boot Method

The two processors have two independent boot copiers; they run sequentially from the same parallel flash, but the different reset address. The first boot copier begins executing when the second processor is reset. After the first process has already boot over, the second boot copier recover from the reset state.

Data Sharing

Dual-port RAM without interrupt control was used which can reduce access latency.

The main control parameters were stored in the dual-port RAM and both the processors separately access the parameters without interrupt signal. In order to prevent the conflict between writing and reading the same data at the same time, the system divides the shared data into two parts, one could only be rewrite by one of the processor. Based on this access structure, one processor can focus on control process, and the other one can focus on communicating process.

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PWM GENERATOR

The PWM frequency ranged from 1kHz to 100kHz by Hardware Description Language (HDL) with 6.67ns step size. The effective resolution of the PWM is related to the output frequency, the Figure 3 Shows the effective resolution of PWM generator.

Rounding Correction (RC) [4] was used to improve the precision of the PWM. When the calculation duty-cycle is not the integer of the minimum step (6.67ns), it removes the mantissa in the current calculation periods and accumulated the mantissa in the next calculation periods. Once the cumulative value reaches the minimum step, add one minimum step to the PWM signal's duty-cycle, and then continue to accumulate.

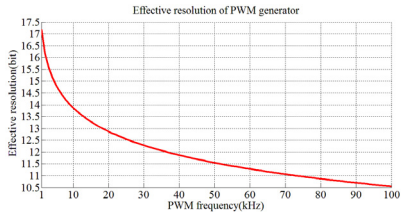

Figure 3: Effective resolution of PWM generator.

HIGH RESOLUTION ADC

All of the ADC channels are synchronized with the PWM's output from the control card. So, the voltage sample rate is equal to PWM's output frequency, which will convert and transmit the value of two voltage signals to the control card separately before the end of every PWM's period. But the current sample rate is fixed, which improves the sample resolution by over-sampling method, the fixed sample rate is integer of the real sample rate. At the initial time of every PWM's period, the current chooses the times of over-sampling before the end of every PWM's period, and transmit the sample data to the control card. So, this synchronous over-sampled method can effectively improve the effective resolution of the current.

In order to confirm the sample resolution and stability, a Calibrator voltage was used as the input signal, the calibrator key parameters are as following:

- Ranges & Accuracy: 0 to 999.999mV in 1μV steps/±0.005% of setting ±0.002% of range.
- Temperature Coefficient: <5ppm per degrees Celsius.
- Long Term Stability: <5ppm/day, <15ppm/90day, <25ppm/year.
- Short Term Stability: <0.2μV/sec, <0.5μV/10sec, <1.5μV/min.

Resolution of the Current Channel

$$\text{Resolution} = \log_2\left(\frac{V_{IN}}{V_{RMS}}\right). \quad (1)$$

The same signal form the Voltage Calibrator was sampled with a different frequency, then calculate the effective resolution of the current channel (see Eq. 1). The V_{IN} is the sampled signal, and the V_{RMS} is the Root-Mean-Square (RMS) noise of the sampled signal.

Figure 4 shows the effective resolution of the CSC. Due to the excellent circuit design and the high precision ADC chip. Even the PWM rate is 100kHz, the effective resolution of the current is more than 18.5.

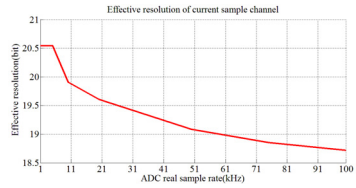

Figure 4: effective resolution of the CSC.

Figure 5 and Figure 6 confirm the high resolution of the current channel of ADC card. The graphs show the digital value for about 1ppm and 2.5ppm input voltage steps.

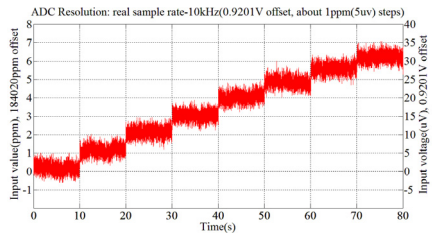

Figure 5: ADC input signal for about 1ppm input voltage steps.

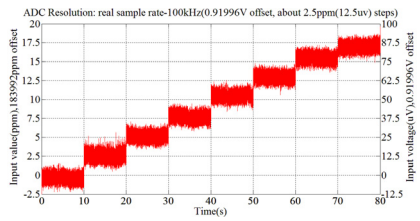

Figure 6: ADC input signal for about 1ppm input voltage steps.

Long-term Stability

Figure 7 shows the test time about 24 hours. The stability is better than 10 ppm.

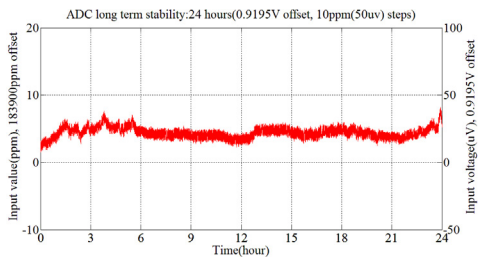

Figure 7: 24 hours stability test.

PROGRAMMABLE WAVEFORM

Some booster ring magnet power supply need output programmable waveform. For the proton boost ring, the

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dipole magnet PS need to output different programmable waveforms in adjacent period during the course of therapy. For the moment, the developed digital controllers are limited by the communication speed and timing design, it is difficult to achieve this requirement.

Thanks to the controller's high speed Ethernet interface and precise timing design, "ping-pang" control method was used. The controller receive the next waveform data in the process of the current waveform output, the high speed communication and dual-processor system make the "ping-pang" control go on smoothly.

The waveform control mode of the digital controller can be divided into "local self-trigger control" and "remote trigger control". In the "local self-trigger control" mode, the controller generate data trigger and period trigger automatically, and control the PS output the periodic and no phase difference waveform; in the "remote trigger control" mode, the user generate period trigger and transmit to controller by optical fiber, and controller generate data trigger automatically.

APPLICATION

In the application of a prototype dipole magnet PS of Proton Cancer Therapy Facility, the current ripple from 1kHz to 10kHz should be less than 1 ppm; in the dynamic case, the PS can be able to output programmable waveform. To realize this high-performance PS, a parallel structure was developed with double closed-loop control system. Figure 8 shows the block diagram of a dipole magnet PS, block A and block B are controlled by two sets of controllers as the slave, and another digital controller control the A and B as the main controller, they connect with each other through high-speed optical fiber.

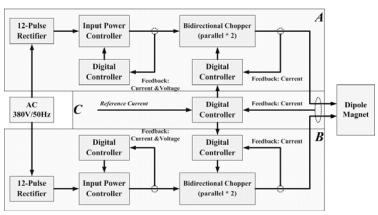

Figure 8: Prototype of dipole magnet PS block diagram.

Ultra Low Current Ripple

Thanks to the controller's precise timing design, through the controllers' accurate phase shift control, the fundamental frequency of the output current is 4 times of the switching frequency, this solution reduce the switching loss of power devices but improve the fundamental frequency of the output. In addition, the double closed-loop control system which controlled by three digital controllers ensure the output precision, long-term stability, and share current. Figure 9 shows the high precision output current of the prototype dipole magnet PS. In the case of the PS output current is 1200A, the current was sampled by a high precision ADC with sample rate of 50kHz. The graph shows FFT analysis of the current.

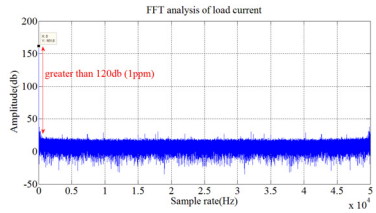

Figure 9: High precision output of the PS.

Programmable Waveform

In dynamic output case, the PS must run to 1200A in 0.75s linearly, and output programmable multiple stepped trapezoidal waveform. Figure 10 shows the dynamic output of the prototype dipole magnet PS. The rise slope is 1715A/s, the fundamental frequency of the output current is 64kHz (controllers' PWM output is 16kHz); the complete output waveform contains 6 steps, 16000 points, every 20 PWM periods trigger one waveform data. It is worth mention about that the output waveform can be adjusted in the next waveform period.

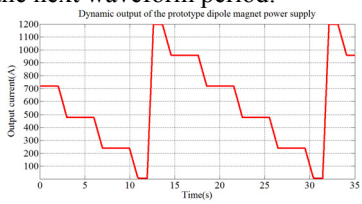

Figure 10: Special dynamic output of the PS.

CONCLUSION

From the application of magnet PS, the developed digital controller is suitable for extremely precise current control. Especially the excellent synchronous control and the waveform control are different from other digital controllers. In addition, the general Ethernet interface is a trend of the digital controller of magnet PS.

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