

A STRIPLINE KICKER DRIVER FOR THE NEXT GENERATION LIGHT SOURCE*

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Abstract

Diversified Technologies, Inc. (DTI) has designed, built, and demonstrated a prototype stripline kicker driver capable of less than 10 ns rise and fall time, ~40 ns pulse length, and peak power greater than 1.7 MW/pulse.

INTRODUCTION

Diversified Technologies, Inc. (DTI), under an SBIR grant from the U.S. Department of Energy, assembled a prototype pulse generator capable of meeting the original specifications for the Next Generation Light Source (NGLS) fast deflector. The ultimate NGLS kicker driver must drive a 50 Ω load (a 50 Ω terminated Transverse Electromagnetic (TEM) deflector blade) at 10 kV, with flat-topped pulses according to the NGLS pulsing protocol and a sustained repetition rate of 100 kHz. Additional requirements of the specification include a 2 ns rise time (10 to 90%), a highly repeatable flat-top with pulse width from 5 – 40 ns, and a fall time (90% to .01%) less than 1 μ s. The driver must also effectively absorb high-order mode signals emerging from the deflector itself.

STRIPLINE KICKER DRIVERS

The ultimate size, and hence cost, of any damping ring strongly depends on the speed of the kickers. It is envisioned that a scintilla of deflection will be imparted by a symmetric pair of shaped parallel deflection blades, pulsed in opposition at 10 kV. Within the guide, comprised of the two deflector blades and their environment, each TEM wave produced by the two pulse generators traverses the guide synchronously with the selected (relativistic) charge packet. Various system designs were explored for producing the desired pulse wave forms. The options included a direct series high voltage switch, solid-state Marx bank, inductive adder, or more conventional pulse transformers and transmission-line adders, several of which were considered in detail. The inductive adder was ultimately selected as the preferred development path for the remainder of the program.

The DTI team has designed and demonstrated the key elements of a solid-state kicker driver capable of meeting the NGLS requirements, with possible extension to a

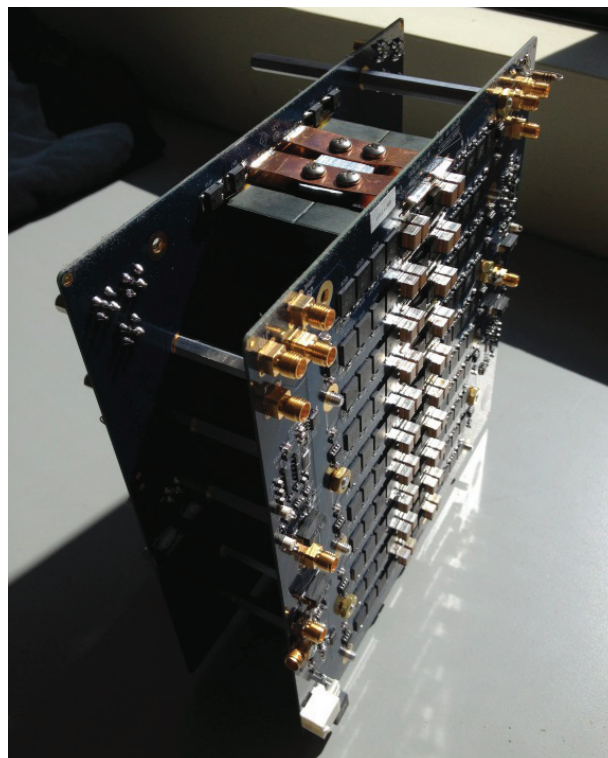


Figure 1: The dual-board pulser, displaying top and bottom boards with central output busbar.

wide range of fast-pulse applications. The current iteration employs compensated-silicon MOSFETs with a charge-pump gate drive arrangement. Two of these transistor-gate driver modules are used to drive opposite ends of the primary winding of an inductive adder transformer in a Marx-derived topology, achieving 1 kV per stage with transistors rated for 650 V. The high voltage gate-drive technique speeds up switching by quickly charging the power transistor gate capacitance in spite of significant internal gate resistance and package inductance. This can be considered a Marx generator-type circuit because two capacitors are charged from the prime power in parallel and discharged in series.

A high performance pulse amplifier is needed to drive the large number of MOSFETs. The pulse amplifier topology is: a Class-A MOSFET inverter; a single-stage MOSFET follower; a MOSFET inverter; and finally a MOSFET follower. The result is a pulse amplifier chain with less than 5 ns group delay and less than 5 ns

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minimum pulse length. Several of these driver chains are used to drive the 80 MOSFETs on each circuit board.

HYBRID MARX-INDUCTIVE ADDER

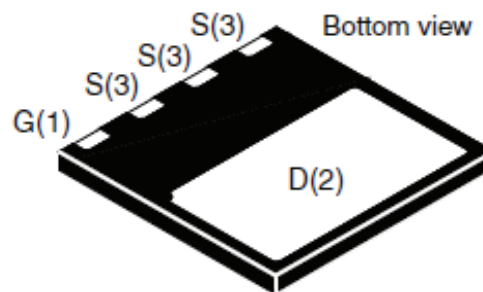
The inductive adder functions by applying several separately-powered primary circuits, each with its own ferrite coupling transformer core, to a single shared secondary circuit. In this manner, the voltages of all the primaries add together, creating one large output pulse. The output pulse voltage is simply the applied voltage, minus any forward drop in the switching circuitry, across the "T" model of the output transformer. The current through the magnetizing inductance is chosen to be very small compared to the main pulse current, perhaps 1/100th of the main pulse current. This way, the clamp diodes across the primaries are not dissipating too much power on each pulse. The transformer leakage inductances then primarily set the rise and fall time of the system. Currently, no efforts have been made to optimize the primary-referred secondary inductances as 7-10 nH was achieved with simple methods.

In Figure 2, the green line shows the flow of current during the "charging" phase. The capacitors C1 - Cn are charged through the resistors to the nominal 500 V bus voltage. The blue line shows the flow of current during the "on" state of the transistors. The various blocking inductances and snubber diodes are not shown in the interest of clarity.

CIRCUIT BOARD LAYOUT

The PCB layout is key to utilizing the low inductance of the transistor devices (Figure 3). The PCB traces are arranged to minimize stray inductance and make the return paths explicit and low inductance. The measured stray inductance of the PCB to the MOSFETs is roughly 1 nH. The package inductance is estimated in the 1 nH range as well. The primary winding has a leakage inductance of 2 nH by calculation. Assuming an

optimized, primary-referred secondary leakage inductance of 5 nH (similar to the primary circuit total inductance), the total inductance between the primary switch and the load is just 10 nH. However, the material used initially for the cores was FerroxCube 3F3 material, which even though it has a reasonable pulse-permeability, appears to be limiting rise time and stressing the transistors with excess magnetizing current. With an ideal load, the pulser shows current rise times in excess of 20 A/ns. The exploration of magnetic materials with superior pulse permeability is an ongoing effort. Optimized core materials will yield rise times closer to the ideal case.



PowerFLAT™(8x8) HV

Figure 3: STMicro PowerFlat 8x8 mm package. This transistor package lends itself well to extremely fast switching and high voltage applications due to its low intrinsic lead inductance.

Optimization of the PCB is similarly important to the ultimate success of this effort, and has required working directly with PCB manufacturers. Future work will rely on iterative improvements of this low-inductance board manufacturing technology.

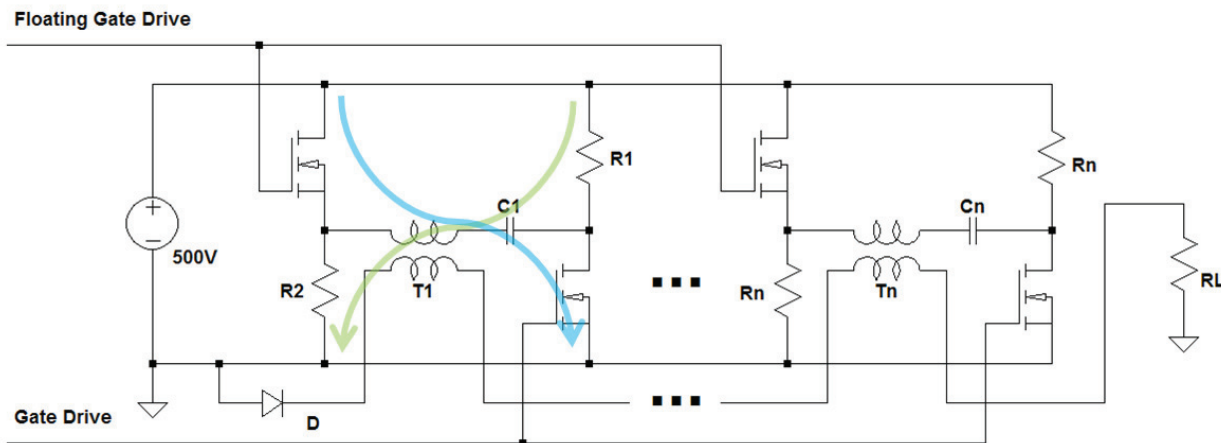


Figure 2: Electrical schematic of two stages showing main pulse current path in blue and charging current path in green. The floating gate drive is referenced to the source leads of the "flying" transistors. For clarity, snubbers and clamp diodes are not shown.

RESULTS

The fully populated (dual-board) pulser with low inductance output structure is shown in Figure 1, while Figure 4 displays pulser performance. Note the arrangement of both sides to drive the common output busbar. The busbar was designed to fit snugly inside the core structure with enough clearance for 6 layers of 0.005" Kapton sheet as insulation. The bar was rounded on the edges to relieve electrical stress on the insulation, but the radius was simply 1/8" instead of an actual Rogowski profile. The output was terminated into 50 ohms with a simple Bourns 50-ohm RF terminator resistor without much regard to the impedance of the structure. Future designs will incorporate some impedance control on the secondary winding.

DEVICE SELECTION

The speed of the SLK module is currently limited by the gate driver chain. Much faster GaN transistors have

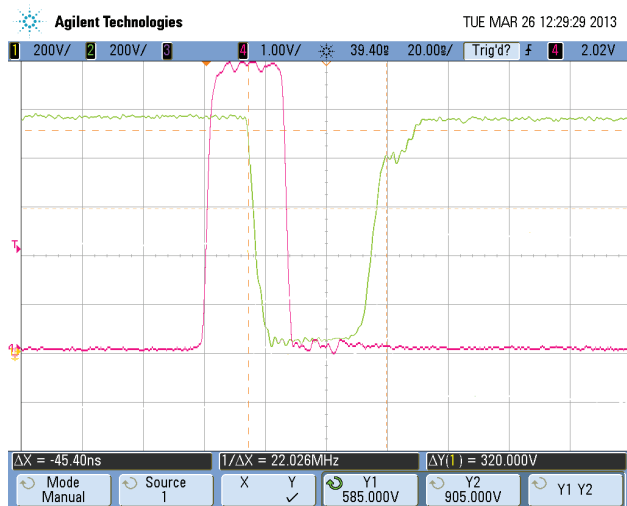


Figure 4: Output of the pulser into 50 Ω . In red, the command pulse is for a 30 ns pulse. The output pulse is stretched slightly to approximately 37 ns, shown in green. The pulse shows 7 ns rise and 7 ns fall into 48.2 Ω , 9250 V peak, 192 A, for a peak power of 1.7 MW/pulse. The slight bump in the fall is due to mismatching of the timing pulses for the MOSFET gates.

recently become available, and simulation of a 5 ns full power pulse with a GaN driver and the best available compensated silicon power devices shows the potential for significant increases in speed (Figure 5).

FUTURE EFFORTS

Within the remainder of the project, effort level will remain high, as the initial challenge of circuit selection and demonstration is over. The hardware to test our theories has been built and proven to the 1 MW level. Testing of the hardware will continue, comparing the results with the initial PSPICE simulations and extending to 2 MW/pulse. Changes will be made to improve rise time and fall time by altering the physical form of the secondary windings and materials of the coupling transformers. Cooling options will be studied, and appropriate adjustments will be made to the design in order to complete a lab-bench prototype of the pulser that will support full voltage and current at the required PRF cooling.

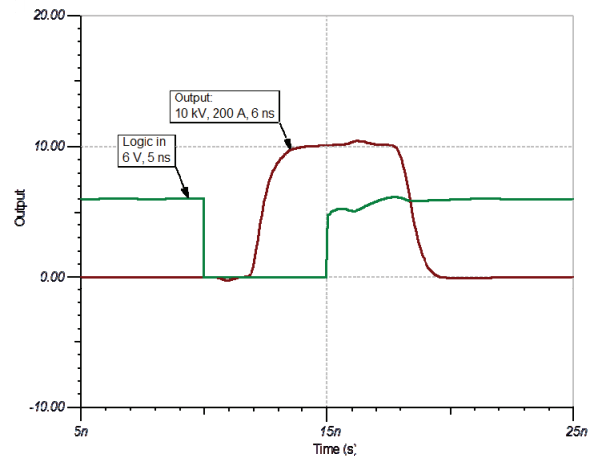


Figure 5: Simulation of two modules in series. It shows much faster rise and fall times (about 1.1 ns) than previously seen or simulated. Pulse width distortion is also much improved—the output pulse is just 1 ns longer than the input.