COMMISSIONING OF THE LOW-NOISE MTCA.4-BASED LOCAL OSCILLATOR AND CLOCK GENERATION MODULE*

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Abstract

Within the Helmholtz Validation Fund Project "MicroTCA.4 for Industry", DESY together with collaboration partners from industry and research developed a compact fully MicroTCA chassis-integrated local RF oscillator module. The local oscillator and clock generation module generates a low noise local oscillator out of the global reference that is distributed over the accelerator. The module includes a splitting section which provides 9 local oscillator signals which are distributed over the RF-Backplane to the rear-transition modules. Similarly, the clock signal is also generated out of a single reference input by means of low-noise dividers. The clock is then fan-out to 22 differential lines that are routed over the RF backplane to the rear-transition modules. The functional block is implemented such that it fits in the rear slots 15 and 14 of a standard MTCA.4 crate. In the paper the commissioning results measured on the L3 low-level RF stations of the European XFEL will be presented.

SYSTEM ARCHITECTURE

The basic RF field detection scheme for the XFEL imposes specific requirements on the local oscillator (LO) and clock (CLK) generation circuits. The main design parameters are large number of tap-points and performance in terms of phase and amplitude stability. The decision was taken that each crate will have its own LO and CLK generation module. If one LO/CLK generation circuit would be serving multiple crates, this would cause issues with cable-drifts and reliability. On the other hand, having one LO/CLK generation circuits per one down-converter unit (8 field detectors) would increase the performance that could be achieved by vector-sum processing gain. The last option will be investigated in the future.

The LO/CLK module presented in this paper is located in the rear side of a standard MTCA.4 crate in slot 15. It uses a dedicated RF backplane [1] for distributing the LO and CLK signals. This reduces the amount of cables needed. The crate environment provides also the power, hardware management and data communication to the module.

One of the main functions of the LO/CLK generation module for the XFEL is to provide the local oscillator (LO) frequency at 1354 MHz. The LO frequency is generated by means of splitters and dividers as shown in Fig. 1.
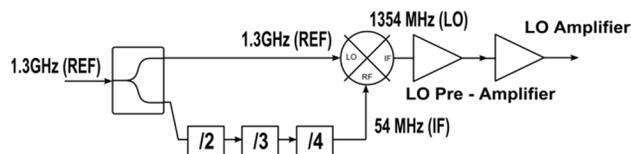
Figure 1: Generation of the local oscillator frequency.

Even if other architectures such as PLL-based circuits cover a wider frequency range of possible LO frequencies the method using dividers-only can practically achieve a lower residual phase noise while keeping the circuit simple. Because of the high number of tap-points the RF power before the splitting has to be in the order of 1 W which represents also a challenge in terms of shielding and DC power dissipation.

The generation of the CLK signals is implemented via simple clock dividers. The reasons for such architecture are similar to the ones for the LO generation.

HARDWARE OVERVIEW

The module is composed of several subsystems. The carrier hosts the RF splitting section, the CLK signal generation, the digital management section, the application processing unit and the low-noise linear regulators. Other functionalities such as DC/DC converters, the temperature controllers and the local oscillator generation are moved off the carrier board on daughter cards and connected to the main board through multi-pin connectors.

Carrier Board

The carrier board's primary function is frequency and clock distribution to the RF back plane (see Fig. 2). The 25 PECL differential clocks can be activated individually. The LO (1.354 GHz), CAL (1.3 GHz), and REF (1.3 GHz) signals are distributed via small 'RF-Mezzanine' cards that are directly soldered to the Carrier. Each RF-Mezzanine card provides a 1:9 signal fan-out as well as individual fixed attenuators and an absorptive RF switch for each signal. By swapping RF-Mezzanine cards frequency distribution up to 6 GHz can be achieved without altering the supporting carrier hardware.

The carrier also provides DC power generation for the system via a shielded 'DC/DC-Mezzanine' card that hosts two 8 A switch-mode convertors. One convertor provides a 5.9 V output used by the numerous LDO's on both RF and carrier card, the other convertor provides a 5.0 V output used exclusively for temperature control via thermoelectric controllers (TEC's) and Peltier elements.

Another individually shielded mezzanine card, the 'TEC-Mezzanine', hosts three independent TEC controllers each capable of 6 A, 5 V Peltier drive. Lastly, the Carrier houses an ARM micro-controller and numerous diagnostics used for system monitoring and control.
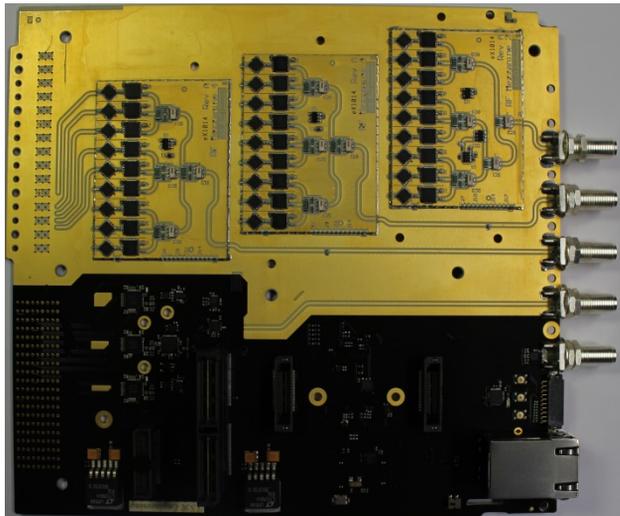
Figure 2: Picture of the carrier-top.

RF Daughter Card

The RF daughter card is shown in Fig 3. The architecture presented in Fig. 1 is implemented on a 6-layer RO4003C/ RO4450F printed circuit board (same stack-up as the carrier board). The main challenge was to choose the components in a way to reduce the residual phase noise to a minimum and at the same time providing 1 W of LO power at the connector. The whole module is enclosed into an aluminium shields on the top and bottom which helps increasing isolation between channels.
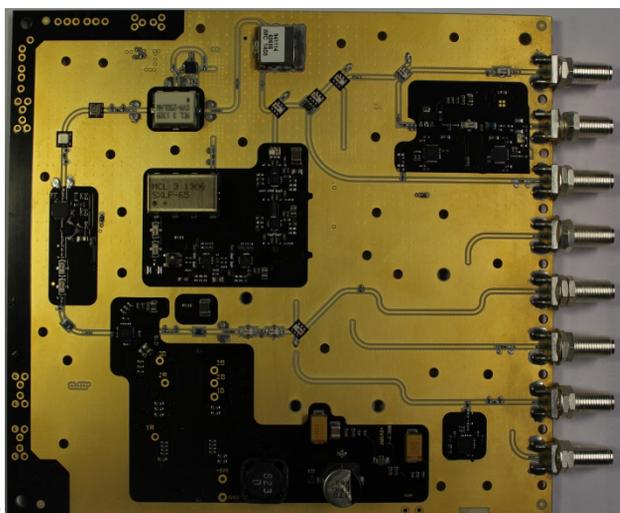
Figure 3: Picture of the RF daughter card-top.

The circuit can be temperature stabilized by means of 3 independent Peltier elements that are controlled from the carrier module. Other features include precise temperature measurements in several points and remote adjustments of

LO power in the range of 3 dB. The full module assembly is shown in Fig. 4.

PHASE NOISE CONTRIBUTIONS

A detailed break-down analysis of all the phase noise sources in the system in Fig. 1 was carried out. The cascade of the dividers was measured to have 3.2 fs residual phase noise and it was assumed to be the highest phase noise contributor. A large market survey was done in order to find the lowest-additive phase-noise dividers. The other significant contributor is the pre-amplifier which can be replaced with a better performance counter-part in the future. The mixer and the output amplifiers are close to the measurement setup limits. The residual phase noise contributions are summarized in the table below. The integration bandwidth for the measurements was in the range [10 Hz – 10 MHz]. The measured values are summarized in Table 1.

Table 1: Residual phase noise of components.

Component	Integrated Jitter [fs]
Test setup	1.3
Cascaded Dividers	3.2
Preamp	3.4
High Power Amp	1.3

The overall residual phase noise is therefore 4.8 fs (4.3 fs with no test setup) in a frequency range [10 Hz to 10 MHz] or 2.3 fs in the integration range from 10 Hz to 1 MHz. The main limitations are the dividers.

GENERAL RF PERFORMANCE

We have focused on evaluating the S parameters, the harmonic content of the output signals and the isolation between various channels.

The general requirement for the return loss was -20 dB (1% of the forward power is reflected) and we managed to meet it on most of the connectors with narrowband matching and proper RF design. The harmonic content was minimized by means of filters to below -80 dBc for the 2nd and 3rd component on all the outputs.

The measured losses are mainly due to material loss because transitions such as vias, main board to mezzanine vias and connector footprints were optimized for maximum power transfer.

There are several potential noise sources such as the DC/DC switch mode regulators and ECL clock fan-outs. By careful layout and shielding of both the noise sources and the RF signals the added noise has been minimized to the extent that the DC/DC switching frequency (500 kHz) does not appear as a peak on the SSA spectrum of the RF outputs - indicating its noise density is below -110 dBv/Hz. By careful shield design, and conductive plating, the cross-talk between the LO, CAL, and REF signals is below -96 dB on any channel-to-channel pair.

The isolation between channels is greatly improved by proper shielding of the RF sections. The sufficient amount of screws and proper contact to PCB GND plays an important role in maximizing isolation.
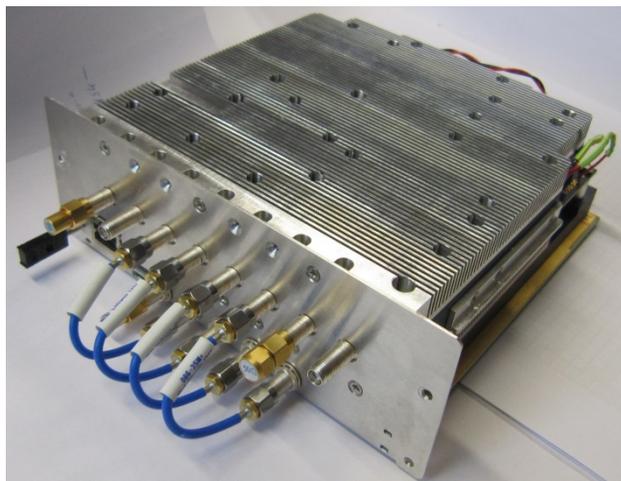
Figure 4: Picture of the fully assembled module.

DIGITAL DOMAIN

As a final tests we integrated the LO/CLK generation module into a standard European-XFEL LLRF station. As a performance test we used a 1.3 GHz source as a reference and fed it into the LO/CLK generation. The same reference was also sampled by the digitizers. We used the SIS8300L2V2 [2] 10 channel digitizer. The acquired data was properly decimated in order to increase the resolution of the FFT. The results are shown in Fig. 5. The y-scale is adjusted to an equivalent 50 ohm analog environment. The main noise limitation is defined by the ADCs and the noise added by the CLK.
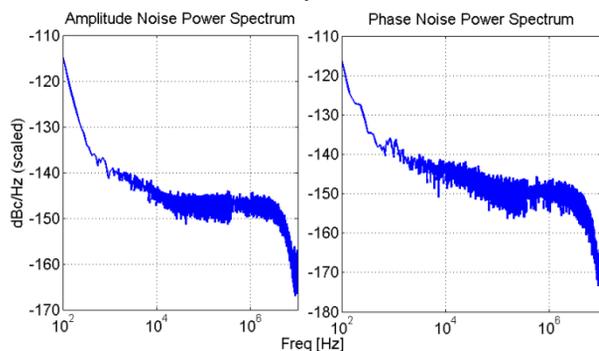
Figure 5: Performance of digital acquisition.

SYSTEM INTEGRATION

Beside RF performance the module takes advantage of the standard MTCA.4 communication and management functionalities. The crate environment offers the standard IPMI management layer for the basic hardware functions (de/activation, health monitoring, events etc.).

The crate environment offers the standard IPMI management layer for the basic hardware functions (de/activation, health monitoring, events etc.). Currently we are providing the payload and management power to the module by means of an additional power supply that is plugged into slot -3 in the rear. Such solution is unmanaged.

The final solution will be using a rear module in slot -1 which will provide full management of all the rear modules. Such solution is under commissioning. Fig. 6 shows the configuration of the LO/CLK module (slot 15) and the rear manager (-1).

Figure 6: System integration.

CONCLUSION

The DRTM-LOG1300 has been successfully tested and used in a European XFEL LLRF station. We will have to install 42 of such modules in the near future.

The full integration tests with the rear manager are in commissioning stage.

REFERENCES

[1] T. Lesniak et al., "Femtosecond Precision via RF Backplane", MIXDES 2013, Poland, 2013.

[2] www.struck.de