ISBN: 978-3-95450-168-7 doi:10.18429/JACoW-IPAC2015-MOPTY071

FPGA BASED GLOBAL ORBIT FEEDBACK IN THE TAIWAN LIGHT SOURCE

C. H. Kuo, P. C. Chiu, K. H. Hu, Demi Li, Y. S. Cheng, K. T. Hsu
NSRRC, Hsinchu 30076, Taiwan

Abstract

The global orbit feedback for the 1.5 GeV electron storage ring of TLS has been operated more than ten years. This system uses general processors to control feedback loop with 1 kHz rate. It is very important for various operation of storage ring now, but some hardware components could have been out of stock in the future. As a prototype, a FPGA based fast global orbit feedback at a 10 kHz data acquisition rate has been developed. A micro-TCA liked platform with FPGA board is used to implement control algorithm and acquire BPM data from Libera Brillance. The correction algorithm is written in VHDL and connected to power supply with AURORA digital links. The system architecture will be discussed in this report.

INTRODUCTION

Orbit feedback system operation of general processors is integrated with Libera Brilliance since 2008. The Brillance supports many beam position functions: slow position data acquisition, post mortem and tune measurement in the TLS. The group topology of Libera Brilliance to acquire fast data at 10 kHz rate has been under testing to verify long-term reliability and stability. The general processors are enough for orbit control. There are two reasons to migrate general processor to FPGA. One, single processor is hard to handle many individual PID control algorithm calculation; another is general cpu platform and operation system that couldn't be upgraded in the future. From maintenance points of view, keep control system of TLS and TPS to be same can reduce this cost. The grouping latency of Libera have been measured and tested that is satisfied for orbit feedback system. It is reliable. The new system is still following this structure. On the other hand, the corrector power supply control is also migrated to FPGA with rocket I/O interface from general cpu with VME bus. Integration of all of the new switching power supplies will be accomplished recently.

THE FPGA BASED FEEDBACK PLATFORM

Feedback System Overview

The TLS Fast Orbit Feedback Application runs in the micro-TCA liked chassis from commercial product. The BPM incoming data comes from the group of Libera Brilliance and is received through the SFP slot (GbE interface) in the GDX module [1]. The FOFB calculations and magnet output are implemented in the GDX module. Global orbit position is concentrated by a group of Libera Brilliance devices. Libera Grouping must be configured as per unit. The FOFB control algorithm runs in two same chassis of GDX, one for horizontal and one for vertical plane. Two Libera Brilliance devices from the group must be selected as master Liberas to output the global orbit position. The general overview is presented in Fig. 1.

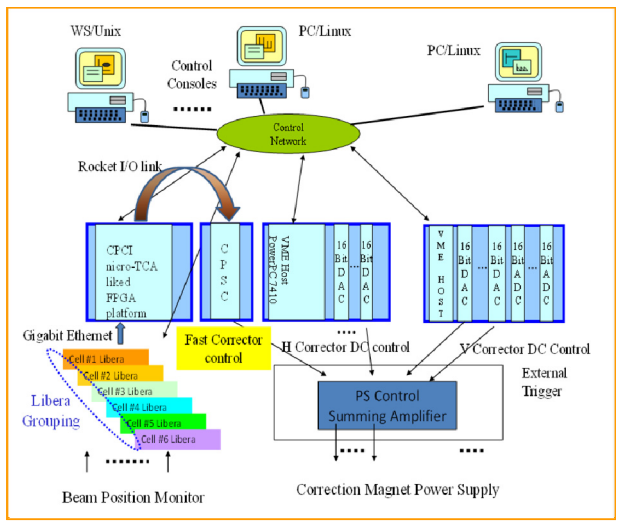

Figure 1: The overview system block diagram.

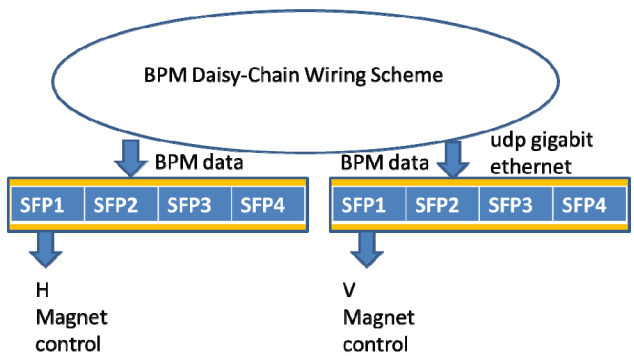

Figure 2: Feednack system is integrated by daisy-chain wiring bus of bpm with GDX module.

The global orbit data packet is received in the GDX of micro-TCA liked chassis, it is written to the circular buffer and it enters the FOFB calculation process which ends with DAC setting output on a SFP1 slot with AURORA 2.5 Gbps duplex protocol. It is then led to the Corrector Power Supply Controller Interface (CPSC) which provides analog output to corrector magnets [2]. The communication block diagram is shown in Fig. 2. The feedback platform photo is presented in Fig. 3.

ISBN: 978-3-95450-168-7 doi:10.18429/JACoW-IPAC2015-MOPTY071

Figure 3: Feednack system platform.

Circular Buffer Data Access

The global orbit data is sent from the SFP2 slot with gigabit Ethernet interface to memory in the GDX module directly. The memory is set-up as a circular buffer and contains the history of around 200 seconds before current time. The gigabit Ethernet is running UDP/IP peer to peer protocol.

There is 59 BPMs in the grouping structure, but 64 BPM ID data is reserved in the circular buffer. Extra buffers will be written to 0 in the each data filling.

The new feedback platform is based on Libera Brilliance+ that is micro-TCA liked system with different kinds of digital bus. GDX (Gigabit data exchange) module is for FA data grouping and FOFB computation.

Magnet Data Output

The magnet data output (M) is set to SFP1. The data is sent using AURORA duplex protocol at 2.5 Gb/s. The data packet contains a 32-bit header (16-bit counter) and magnet data. Each magnet data contains 1 bit for identification of the magnet type (horizontal/vertical), 7 bits for its ID and 20 bits for DAC setting. Correctors setting is sent in a packet (all together in series).

CORRECTOR POWER SUPPLY CONTROL INTERFACE

The corrector power-supply controller interface (CPSC) is based on Xilinx Spartan-6 FPGA. It was contracted to D-TACQ. This module will convert dgital data to 16bit analog output from AURORA rocket I/O receiving. This CPSC module supports fast settings from orbit feedback system and summed with slow setting from the existed VME ILC. The functional block diagram of CPSC is shown in Fig. 4.

The CPSC includes of 32 channels analogue output and offers substantial performance improvement on RTM-AO16. There are two CPSCI to serve 64 channels of corrector settings. One is master board outputs channels 33-64 and the other is slave board outputs channel 1-32. Master board is auto-configured when SFP attached. The communication of master and slave is through Digital IO by the high density connector (SCSI-II type). The CPSC instrument photo is shown in Fig. 5.

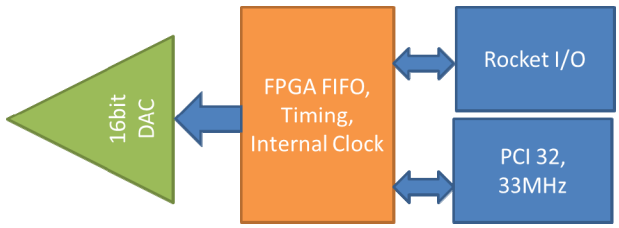

Figure 4: Functional block diagram of the corrector power supply control interface module. T. The fast setting from feedback engines will sum with slow setting from ILC.

(a)

(b)

Figure 5:(a) CPSCI AO32 frontend. (b)CPSCI AO32 backend. 32 channels AO is extend to 64 channels AO by RTM-AO16 bus.

CONTROL ALGORITHM PROCEDURE

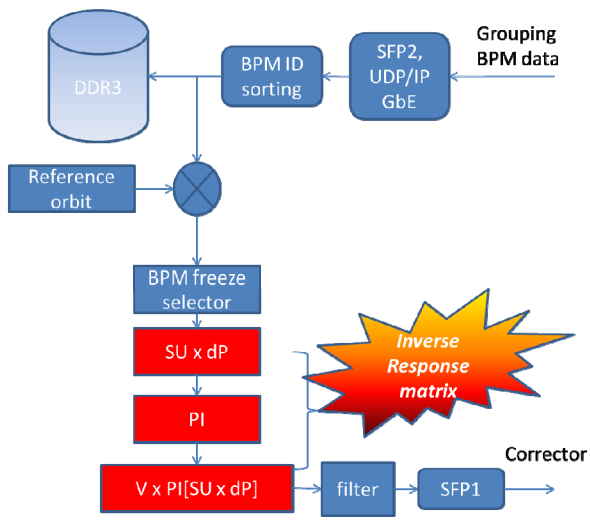

Figure 6: Control algorithm block diagram.

The control algorithm still adopted PI controller. After feedback controller receives bpm data, the XILINX Virtex 6 of GDX plays the control algortithm calculation. The inverse response matrix define model of storage between bpm and corrector. Originally, inverse response matrix processing is PIxVxSUxdP. The new system PI has been inserted in the matrix, between V and [SUxDP]. It means that new system is support to individual PI parameter adjustment with difference eigen-mode of inverse response matrix. The PI block is also vector. The block diagram is shown in Fig. 6 [3, 4].

ISBN: 978-3-95450-168-7 doi:10.18429/JACoW-IPAC2015-MOPTY071

CONCLUSION

Infrastructure of the new orbit feedback system is being implemented gradually without interrupt of the routine operation of the TLS. Individual PI parameters can be applied in the new system. Diagnostic functions by using 10 kHz rate will be also supported along with the new orbit feedback system. A built-in diagnostic function which stores data at higher sampling rate and has hardware and software trigger is to build. All major work, is constrained by available machine shutdown interval, more functions testing will be completed in later 2015.

REFERENCE

[1] http://www.i-tech.si
[2] http://www.d-tacq.com
[3] Pei-Chen Chiu, et al., “TPS BPM Performance Measurement and Statistics”, Proceeding of IBIC 2012, Tsukuba, Japan.
[4] C. H. Kuo, et al., “BPM System and Orbit Feedback System for the Taiwan Photon Source”, Proceeding of ICALEPCS 2011.