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NEW BUNCH-BY-BUNCH FILLING PATTERN MEASURING SYSTEM AT ELSA

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Abstract

The electron accelerator facility ELSA at the University of Bonn, Germany, can accelerate and store electrons with a final energy from 0.8 GeV up to 3.2 GeV. To routinely determine the filling pattern in the storage ring, a new measuring system has been developed. For hadron physics experiments the filling pattern, which is influenced by the injection from the pre-accelerating synchrotron, should be as homogeneous as possible. The new measurement system should provide a real-time measurement of the filling pattern, so that the injection can be continuously optimized. Moreover, a position measurement for each individual bunch is provided, from which the two transverse and the longitudinal tunes can be deduced. To measure the bunch-by-bunch intensity and position, the signals of the existing button-type BPMs will be digitized by fast 12-bit ADCs synchronized to the 500 MHz ELSA radio frequency. The fast pre-processing and intermediate storage of the data is realized with a 500 MHz clocked FPGA and transfers the data to a PC for further processing. First results of measurement system developed in-house will be presented.

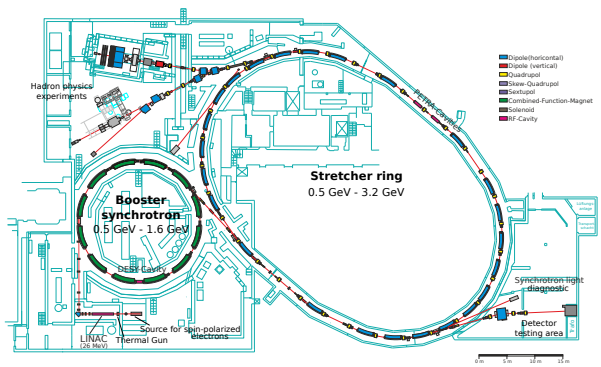

Figure 1: Overview map of ELSA.

THE ELSA ACCELERATOR

The electron accelerator ELSA (short for **El**ectronen **S**tretcher **A**nlage, *English: electron stretcher facility*, overview map is shown in Fig. 1) consists of three accelerator stages: the linear accelerator, the booster synchrotron and the stretcher ring, giving the entire facility its name. In the stretcher ring, a electron beam with a beam energy between 0.8 GeV and 3.2 GeV and a total beam current typically up to 30 mA, can be stored for minutes or up to hours and be extracted to one of the two hadron physics experiments or to the detector testing area. In the booster synchrotron and in the stretcher ring, the electrons are accelerated by 500 MHz cavities, leading to a bunched beam structure with 2 ns bunch separation.

To measure the beam position, a system of 32 Beam Position Monitors (BPM) has been installed in the beam pipe. Until now the electrodes are read out slowly, indicating that only the average position of the beam can be determined with a frequency of 1 kHz. More information can be found in [1].

MOTIVATION FOR A NEW BPM-READOUT SYSTEM

Because of the slow processing of the analog electrode signals, information about individual bunches is not available. This allows a lower sampling frequency and fewer data points are recorded.

A BPM consists of four button electrodes isolated from the beam pipe arranged around the center of it. While a ultra-relativistic bunch of electrons is passing the BPM, a charge is induced on the electrodes, whereby the corresponding voltage can be measured via a resistor. For a beam pipe with infinite conductivity, the induced signal depends on the BPM geometries, the bunch position and the beam filling pattern, i.e. the charge per bucket. This electrode signal, containing information about each individual bunch, is shown in Fig. 2. After 2 ns the signal amplitude is negligibly small, indicating no signal interference between two consecutive bunches.

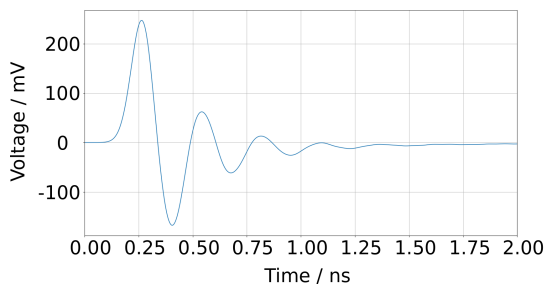

Figure 2: Example for a voltage signal induced by a bunch containing 37 pC charge and a length of 15 mm, corresponding to a beam energy of about 1.7 GeV (see [2]), on the electrode, simulated with the wakefield solver of CST-Studio [3].

In the new readout system, the information for the individual bunches is preserved by a proper pre-processing of the analog signal and the digitization. It is mandatory that the bandwidth of the used components must be large enough and the sample frequency must be sufficiently high. Due to information preservation, the position for all individual bunches, the beam filling pattern and also the tunes in the horizontal, vertical and longitudinal direction, respectively, can be deduced.

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CONCEPT OF DIGITIZATION

The digitization is divided into three stages, shown in Fig. 3. The four analog signals from the electrodes must be pre-processed, after which they can be digitized with a sampling ADC. The digitized signals are further processed

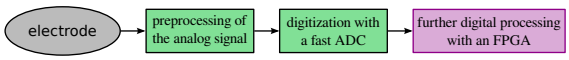

Figure 3: Signal path of the BPM electrode signal to the FPGA.

with an FPGA in such a way that they can be transferred to the control system via a PC. With the new readout system, a single-bunch resolution should be achieved. All information required to calculate the charge and the position can be derived from the amplitude of the electrode signals induced by the bunch. Therefore, it is sufficient to only sample the four signals every 2 ns at the maximum amplitude for an optimal signal-to-noise ratio. In addition, the slope at this point is zero, reducing the impact of timing jitter. Thus, two individual measurements are needed. On the one hand the actual sampling of the signal amplitude and on the other hand the determination of the time offset of the maximal signal amplitude, to adjust the delay, must be performed. Basically, the same electronics can be used for both measurements, shown in the block diagram in Fig. 4.

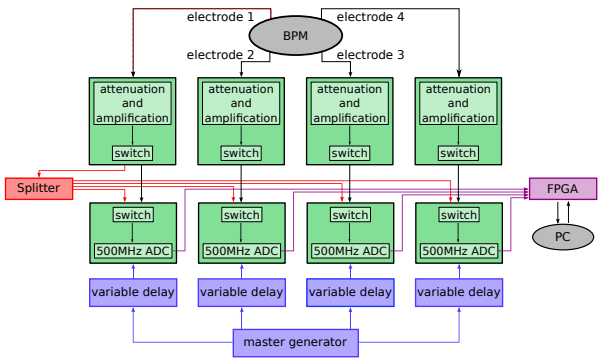

Figure 4: Concept for the digitization.

There are four equal digitization channels for the four electrodes. The pre-processing is shown in the first green box, where the analog signals are amplified or attenuated. To digitize the amplitude of the electrode signals, the amplification stage and the digitization stage, which includes a fast ADC, are connected to each other via the two switches. The ADCs get a clocking signal from the master generator, which provides the 500 MHz signal for the accelerating cavities in the stretcher ring. The clocking signal is delayed with a variable delay to sample the signal at the maximum amplitude. The sampled values are forwarded to the FPGA, which takes over the communication with the PC.

To correctly set the delay on the clocking signal, the second measurement is required, which basically is already implemented within the existing digitization channels. The only additional component is a splitter. The signal from one electrode is divided into four equal signals by connecting one switch not directly to the ADC, but to the external splitter. The other three electrode signals are not used for this type of measurement. The split signals are fed into the four digitization channels, so that each ADC is supplied with the same analog input signal. In this case, the time delay compared to the master generator signal is slightly adjusted for each of the ADCs, to sample the same signal at four different times. This allows the determination of the relative temporal position of the maximum amplitude to the clocking signal, by fitting a derived Gaussian function to the four sample points. From this, the delay for the amplitude measurement can be deduced.

HARDWARE IMPLEMENTATION

The concept described above has been implemented in hardware with two main circuit boards developed in-house, separating digitization from pre-processing. This has the advantage that amplification can take place as close as possible to the electrodes and the digitization can be situated distant to the high radiation exposure in the accelerator tunnel. A Xilinx Virtex-7 FPGA on the VC707 evaluation board connected via adapters developed in-house to the Attenuation and Amplification Board and the Digitization Board is used to further process the ADC data and control the ICs.

Attenuation and Amplification Board

The pre-processing board is set up as shown in Fig. 5. For

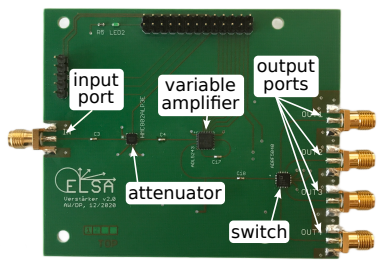

Figure 5: Attenuation and Amplification Board.

different accelerator settings, the input signals of the boards cover several orders of magnitude. Therefore, the first component on the board is an attenuator (HMC802ALP3E from Analog Devices), which can be digitally controlled to 0 or 20 dB. The variable amplifier ADL5243 by Analog Devices with a fixed amplification gain of 20 dB and a variable attenuation from 0 to 31.5 dB, with a step size of 0.5 dB is used to adjust the signal amplitude to the input voltage range of the ADC. In addition, the switch ADRF5040 by Analog Devices has been installed, to switch between the two measurement methods. Currently, only two of the four outputs are used, but to provide more flexibility for the future the installed switches have four outputs each.

Digitization Board

The Digitization Board, shown in Fig. 6, obtains the signal from the Attenuation and Amplification boards along with

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the clocking signal for the ADC. Here, also an ADRF5040

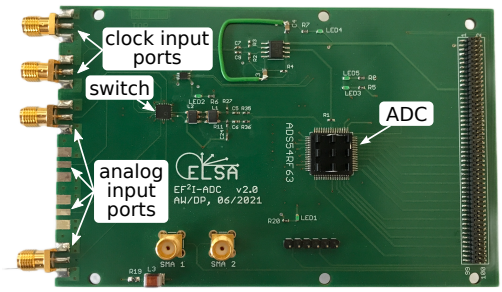

Figure 6: Digitization Board.

switch is used. The ADC ADS54RF63 from Texas Instruments, with a maximum sampling frequency of 550 MHz, is used for digitization. This ADC needs a differential clocking signal. Therefore, an SN65LVDS100 by Texas instruments has been installed, transforming the single-ended clocking signal from the master generator into a differential one.

FPGA Configuration

The Xilinx Virtex 7 FPGA has been configured as shown in Fig. 7. The four digitization channels are also structured

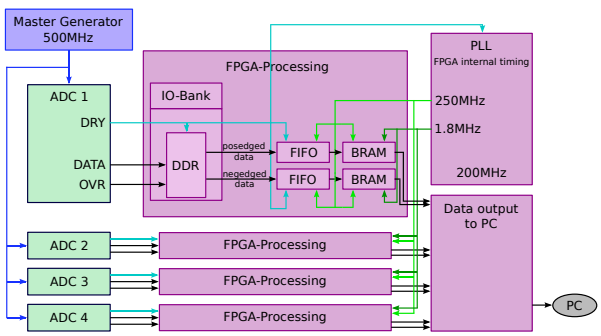

Figure 7: Block circuit diagram of the FPGA configuration.

in parallel to each other in the implementation in the FPGA, ensuring a fast processing. The data from the ADC is sent synchronously with the data ready (DRY) signal on both the positive and negative edges. This results in the DRY signal having a frequency of 250 MHz. The data signal is divided by reading out the positive or negative edge of the DRY signal, whereby two data points are always processed in parallel at 250 MHz.

Before sending the data to an analysis PC, it must first be buffered and the processing frequency slowed down. The FPGA communicates with the PC and also controls the electronic components on the circuit board.

MEASUREMENTS AT ELSA

With the new readout system, the filling pattern of the electron beam, i.e. the charge of all individual bunches, can be measured. At the time of the measurement, only one digitization channel had been set up, so only a charge measurement was possible and the delay must be adjusted manually. For this purpose, the amplification board was connected to one BPM electrode in the accelerator tunnel, while the digitization board and the FPGA were housed in a radiation-protected location. The plot in Fig. 8 shows the charge in each individual bucket, deduced from the digitized maximum amplitude of the electrode signal and the total beam current, that is also measured. The plot shows three

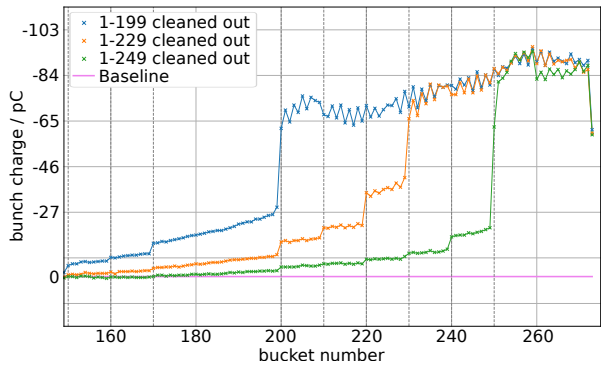

Figure 8: Plot of the bunch charge for the buckets 150 to 274 for different filling patterns.

individual measurements, in which an increasing number of bunches were excited in such a way that they are removed from the electron beam. The excitation happens in sequences of 10 consecutive bunches, which explains the step pattern in the plot. For each measurement, the electron beam only changes due to the reduction of bunches, so the bunches that were not leaving the beam should show the same charge in all three measurements. Nevertheless, between bucket 250 and 260 a decrease in bunch charge can be observed, which is probably caused by the bunch cleaning process.

SUMMARY

A first measurement with one channel of the new BPM readout electronics successfully provided information about the filling pattern in the stretcher ring. The extension to fully use with all four channels is in progress. It will also enable a bunch position and tune measurement. A more detailed description of the readout system and further measurements can be found in [4].

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