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# DIGITAL LLRF FOR THE CANADIAN LIGHT SOURCE

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*Abstract*

The Canadian Light Source, at the University of Saskatchewan, is a 3rd generation synchrotron light source located in the city of Saskatoon, Canada. The facility comprises a 250 MeV LINAC, a full energy booster and a 2.9 GeV storage ring. The radiofrequency system in the booster consist of two 5-cell cavities feed with a single SSPA. The analogue LLRF for the booster has been recently replaced by a digital LLRF based in the ALBA design with a Picodigitizer, a stand-alone commercial solution provided by Nutaq. Also, the firmware of the new DLLRF is configurable to allow operation with a superconducting cavity feed with one amplifier, thus providing the possibility to replace the CLS SR LLRF as well. The main hardware components, the basic firmware functionalities and the commissioning measurements of the new DLLRF for the CLS booster will be presented in this paper.

## INTRODUCTION

The CLS was first funded in the University of Saskatchewan in 1999. After a short period of construction and commissioning, operation for users started in 2005. The SR is a 2.9 GeV machine of 170.88 m long. It consists of 12 double bend achromat (DBA) cells. A 500 MHz radiofrequency system restores the energy of the electrons by means of a CESR-B superconducting cavity feed with a 300 kW klystron. [1,2].

The CLS booster is a full energy synchrotron of 102 m length. The lattice consists of a modified 28-fold supersymmetric FODO lattice that provides the required space to install the two DORIS-type 5-cell cavities in one straight section [3]. A beam up to 10 mA is captured from the LINAC and accelerated to nominal energy with a repetition rate of 1 Hz.

A single SSPA able to provide up to 100 kW feeds the two cavities of the booster. After a high power isolation circulator, the power is split in two branches with a magic-T. The cavities were first installed at the proper distance to assure the right phase difference between them. Nevertheless, a phase shifter at each branch is used to assure this condition, since the phase in the cavities cannot be controlled individually with the LLRF.

In order to replace the analogue control system in the CLS booster, a new DLLRF has been developed based in the ALBA design which was implemented at SIRIUS [4] and modified in order to be able to drive two 5-cell cavities with two plunger each feed by a single SSPA.

Also, the ALBA DLLRF design has been modified to meet the CLS SR requirements, i.e., to be able to drive one or two superconducting cavities with one or two amplifiers. This will allow to install the new DLLRF in the SR also.

## HARDWARE

The main DLLRF components are:

- Picodigitizer: FPGA mother board + FMC boards for ADCs and DACs + mezzanine Mestor with digital GPIO bus.
- Front Ends: RF signals down-conversion, RF drives up-conversion and LO generation with MO reference.
- Digital Patch Panel: Connectors and voltage level conversion between DLLRF and RF plants sub-systems.
- Level translator: CLS designed hardware for extra voltage conversion and electrical isolation.
- Power Supply Unit: Supplies for the active components of the DLLRF.

All DLLRF hardware components, except for the PSU, have been allocated inside an EMI rack (see Fig. 1).

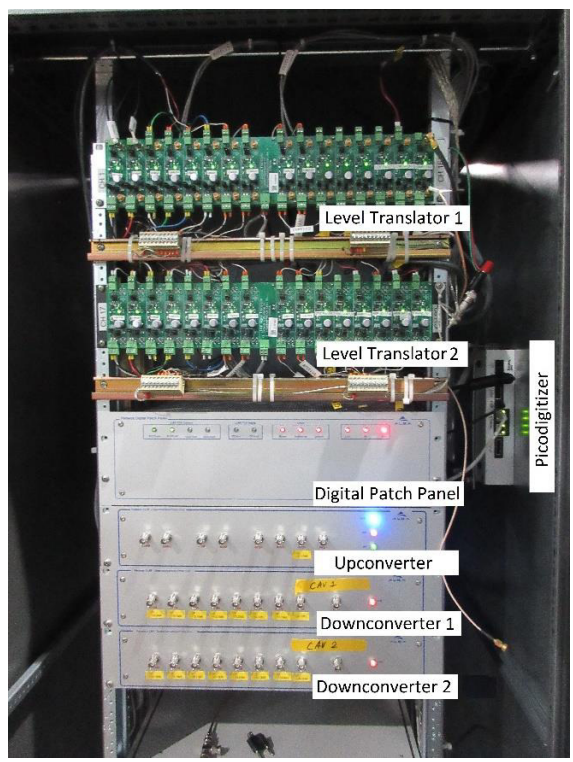


Figure 1: DLLRF components inside the EMI rack.

### *Picodigitizer*

It is a stand-alone board solution provided by Nutaq, that contains a Virtex-6 SX315T FPGA and two FMC boards, one with 16 ADCs channels of 14 bits capable to operate up to 125 MHz and another with 8 DACs of 16 bits up to 250 MSPS. The resolution of the ADCs is better than 0.06 % rms in amplitude and 0.04 º rms in phase. The SNR is better than 70 dB [5].

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A digital interface mezzanine board is also included, the Mestor Breakout Box. It provides up to 32 GPIO used for driving external RF components such as motor controllers, pin diodes and LLRF interlocks outputs or receiving digital inputs from vacuum controllers or external interlocks.

### *Front Ends*

The down-converter front end transforms the incoming 500 MHz RF signal into a 20 MHz IF signal by means of a mixer and a 480 MHz Local Oscillator (LO). The IF signal is sent then to the ADCs.

Isolation between IF channels in the down-converter crate was found to be limited due to crosstalk in the LO distribution splitter. Adding an 8 dB attenuator while maintaining the specified input levels to the mixers increased the isolation. Final measured isolation was >77 dB as measured at the down-converter IF channels. Figure 2 shows the scheme of the LO distribution inside the down-con-verter crate.

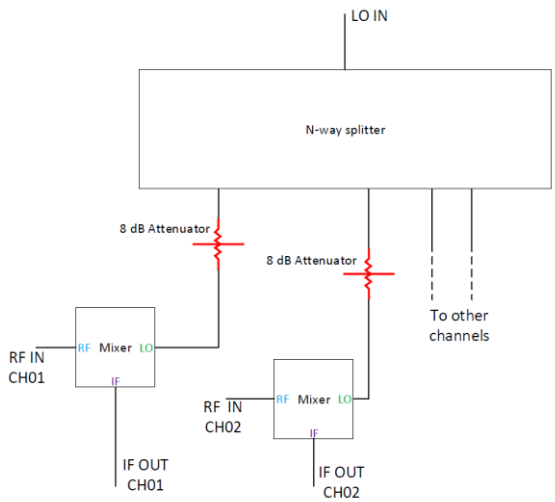


Figure 2: Down-converter LO distribution scheme with new attenuators highlighted in red.

The up-converter crate transforms the IF signal from the DACs to the required RF signal. It also allocates the Voltage Controlled Oscillator (VCXO) needed to generate both the IF and the 80 MHz clock signal to be used for FPGA sampling, thus assuring the proper condition for the IQ demodulation. The VCXO is phased locked with a 10 MHz reference signal provided by the facility. The pin diodes for fast RF drive cut off are allocated also in the up-converter crates.

### *Digital Patch Panel and Level Translator*

GPIO coming from Mestor board signals are split and merged in several connectors in order to be sent to appropriate RF sub-system in the Digital Patch Panel crate.

In addition, CLS designed and built a level translator to convert between different voltage levels such as LVTTL, TTL or 24 V. The level translator provides also electrical isolation.

## FIRMWARE

### *Cavities Configuration*

DLLRF can be configured for three different operating modes:

- Mode 1: Two single-cell cavities feed either with one transmitter each or one for both.
- Mode 2: One single-cell cavity with one high power transmitter.
- Mode 3: Two 5-cell cavities with one high power transmitter.

1st and 2nd configuration allow CLS to upgrade the SR LLRF system with option to install a new superconducting cavity in the SR feed with the existing amplifier or with a dedicated one. 3rd mode is the current CLS booster configuration.

### *Chains*

Two independent virtual cavities, hereafter referred to as chain A and chain B, have been implemented in the firmware and allow the operation of the different modes; specially for modes 1 and 3, in which two cavities must be controlled with one single amplifier. In these configurations, the amplitude and phase loop is computed in chain A and is responsible for the drive generation towards both cavities, whereas the tuning loop and the interlock handling for each cavity is computed in the correspondent chain.

### *Amplitude and Phase Loop*

The DLLRF allows the user to choose between different input signals to be controlled: Cavity 1 voltage, Cavity 2 voltage, SSPA Forward power or the vector sum of Cavity 1 and Cavity 2. This last option is the one chosen for nominal operation at CLS. A digital phase shifter has been implemented on each cavity signal reading in order to add both amplitudes in phase and avoid destructive additions of the total voltage as shown in Fig. 3.

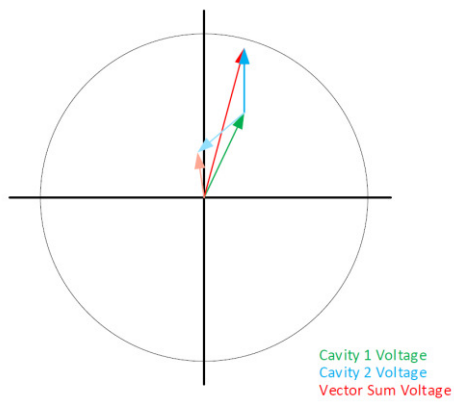


Figure 3: Vector sum of cavity 1 and cavity 2 voltages for different phase shifters in cavity 2.

An extra digital phase shifter has been implemented for the total vector sum and for the rest of signals to be controlled to avoid positive feedback instabilities in the loop.

Loops can either be set to IQ rectangular loops or polar loops.

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### *Fast Interlocks*

DLLRF implements a supervision in all the RF input signals. If a certain level is reached, the interlock is set and latched. The interlock is propagated then by means of digital output towards different subsystems. Particularly to the pin diode, that is opened in less than 1 us. The interlock threshold is adjustable by the user.

The end switches of the plungers in the cavities are also monitored. Finally, a manual alarm can be generated by the DLLRF and trigger an interlock condition as well.

All of the interlocks can be disabled and also a timestamp is provided in order to arrange up to 8 different interlocks in time.

When an interlock is detected, the systems is set to a safe mode in which the drive is decreased and the loops are disabled. A manual reset is required for the interlock condition to be cleared. If more than two cavities are controlled with a single drive, interlocks in both cavities will open the pin diode.

### *Slow Interlock*

The system provides a specific digital input that will trigger the slow interlock. In this case, before opening the pin diode, the DLLRF drops the drive according to an adjustable time value. Only when the minimum drive has been reached, the pin diode will be opened. A 50 ms slow interlock event can be observed in Fig. 4.

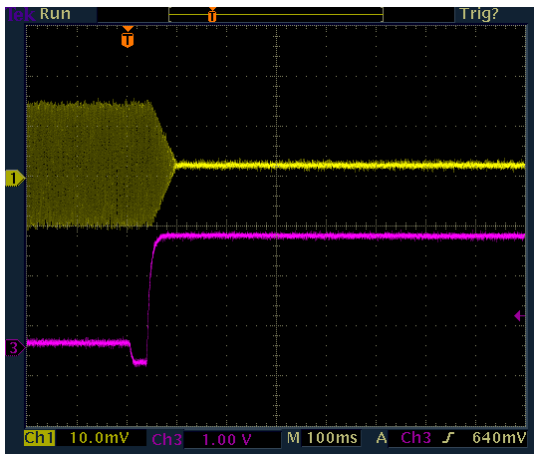


Figure 4: Slow interlock. Yellow: RF envelope. Pink: Interlock trigger.

### *Booster Ramping*

CLS booster is ramping at 1 Hz according to a specific profile defined in Table 1.

Table 1: Ramping Time Parameters

| Stage | Time [ms] |
|---|---|
| Bottom | 166 |
| Rising | 306 |
| Top | 183 |
| Falling | 216 |

All the ramping parameters such as bottom and top amplitude and phase and the rising and falling time, are adjustable by the user. Figure 5 shows the maximum and minimum nominal power of the CLS booster achieved with the new DLLRF system, which are 52 kW and 350 W respec-tively, thus meaning a nominal operation dynamic range of more than 21 dB.

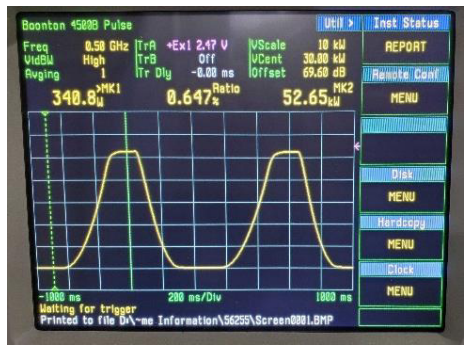


Figure 5: Booster ramping. Yellow: RF envelope.

When the ramping is first triggered, the top level is increased progressively according to a user adjustable setting, so that the total rms power sent to the cavity is also slowly increased.

Tuning and field flatness can be enabled only for the top of the ramp.

## CONCLUSIONS

The DLLRF for the booster CLS, based in the ALBA system, has been successfully installed, commissioned and adjusted for nominal operation in the facility.

It has been demonstrated the feasibility of the system for injection according to CLS nominal operation. Figure 6 shows the capture of the beam in the booster and extraction to SR at high energy, together with RF power for two consecutive injection cycles.

The flexibility of the system will allow CLS to install the DLLRF also in the SR.

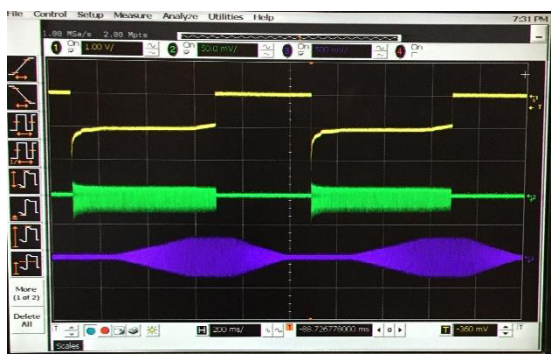

Figure 6: Booster injection. Yellow: Parametric Current Transformer; Green: Fast Current Transformer; Lilac: RF envelope.

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