ISBN: 978-3-95450-227-1 ISSN: 2673-5490 doi:10.18429/JACoW-IPAC2022-TUPOPT067

DEVELOPMENT OF A TRIGGER DISTRIBUTION SYSTEM BASED ON MicroTCA.4

H. Maesaka[†, 1], T. Inagaki[1], RIKEN SPring-8 Center, Sayo, Hyogo, Japan
N. Hosoda[2], E. Iwai[2], T. Ohshima[2], JASRI, Sayo, Hyogo, Japan
[1]also at JASRI, Sayo, Hyogo, Japan
[2]also at RIKEN SPring-8 Center, Sayo, Hyogo, Japan

Abstract

We designed a trigger timing distribution system for MicroTCA.4-based (MTCA.4) electronics and developed a new advanced mezzanine card (AMC) and a level converter module for this purpose. A trigger signal is transmitted through a high-speed serial data stream in an optical fiber. This AMC has five optical transceivers, one for receiving trigger signals from upstream and four for fanouts to downstream. A master AMC distributes trigger timing signals, trigger counts, and event data and slave modules generate trigger output signals with appropriate delays according to the received event data and the local setting for each output channel. The trigger timing of each output can be precisely adjusted with the interval of 509 MHz or 238 MHz clocks. The timing can also be fine-tuned by ~80 ps tap delay. The timing jitter was measured to be approximately 40 ps std., which is significantly smaller than the clock period of the reference clock and sufficient for most applications. The developed trigger system has been utilized in SPring-8, SACLA, and NewSUBARU, and various accelerator components are synchronously operated with sufficient timing accuracy.

INTRODUCTION

A particle accelerator has many components that need precise synchronization among them, such as electron and ion sources, pulsed rf sources, pulsed power supplies, beam diagnostics, etc. The control sequence of these components is getting complex and the data amount is also increasing thanks to the evolution of control and data acquisition electronics. MicroTCA.4 (MTCA.4) [1] is one of the electronics platforms to process large-volume data and it is employed in many accelerator facilities.

In the third-generation light source, SPring-8, for example, the electron beam injector was switched from the combination of linac and booster synchrotron to the linac of the x-ray free-electron laser (XFEL), SACLA [2]. To inject an electron beam in parallel with XFEL operation, the accelerator components must be controlled shot-to-shot by an intelligent triggering system. Therefore, we developed a trigger signal distribution system based on MTCA.4 to synchronize the accelerator components and generate flexible trigger signals for complex operation sequences.

This trigger system was installed into SPring-8, SACLA, and NewSUBARU [3]. The new 3 GeV light source "NanoTerasu" in Tohoku, Japan [4], also employed this trigger system. In this article, we describe the design and performance of the trigger signal distribution system.

DESIGN

Requirements

Since the distance between accelerator components can be in kilometer order, it is hard to transmit high-speed signals through a long metal cable. Therefore, the trigger signal should be distributed by fiber optical links. More than 10 trigger outputs are necessary on the front panel, backplane, and Zone 3. Some signal inputs are also needed for trigger inputs and some other controls. The trigger signal must be synchronized to the acceleration rf frequency of 509 MHz or 238 MHz used in SPring-8, SACLA, NewSUBARU, etc.

Since most of the accelerator components are also synchronized to the power line frequency of 50 or 60 Hz, the trigger signal should be generated with this repetition rate. We call this as a master trigger. The timing of the trigger signal from each output channel should be precisely delayed for up to 20 ms (period of 50 Hz) from the master trigger. The resolution of the timing control should be 0.1 ns level and the jitter should be well below 0.1 ns std. for precise timing adjustment within the acceleration rf period. The trigger output should be turned on or off shot-to-shot according to a given output pattern.

Some frequency-divided signals from the acceleration rf clock are also demanded, such as a revolution clock of a storage ring, for example. Some asynchronous triggers unrelated to the accelerator repetition rate are also needed. By generating an asynchronous trigger from an alarm signal, we can take data from various components at this alarm, which can be useful for postmortem analysis.

Since each accelerator component requires a different trigger input level, the trigger system should deliver appropriate levels of trigger signals. Some components may accept only single-ended signals and some may need differential signals. Since an MTCA.4 board is difficult to generate various output levels and cope with various connector types, an additional interface module is needed.

Trigger Signal Distribution

Based on the requirements described above, we considered the concept of the trigger system. The schematic diagram of the trigger distribution network is shown in Fig. 1. The trigger signal is generated and distributed by a newly developed MTCA.4 advanced mezzanine card (AMC). The master module of the trigger AMC receives an external master trigger signal (60 Hz maximum) and the trigger signal is embedded in a high-speed serial data stream and transferred by optical fibers. The trigger AMC was

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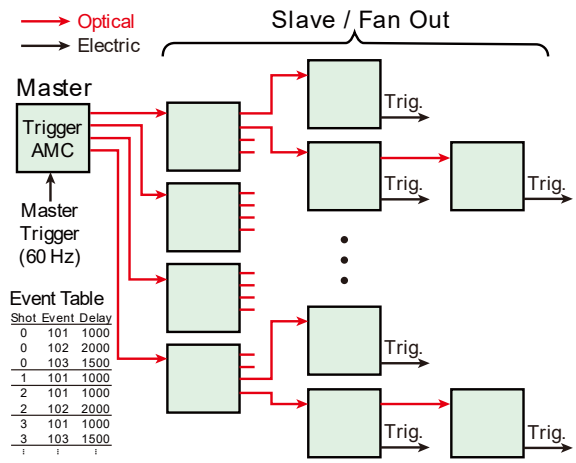

Figure 1: Schematic diagram of the trigger signal distribution system.

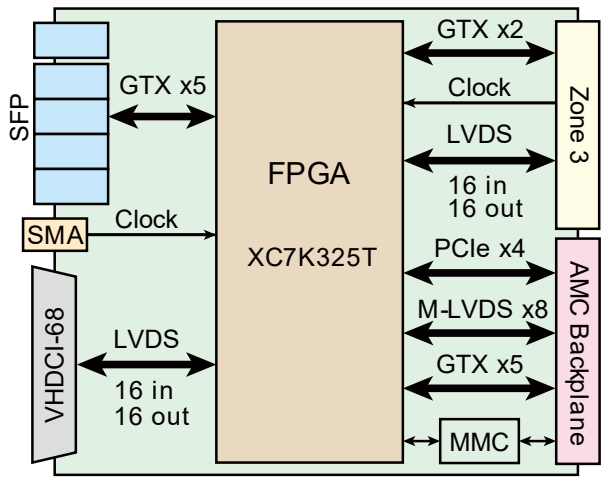

Figure 2: Block diagram of the trigger AMC.

designed to receive one optical trigger signal and transmit four copies of the signal. Each trigger AMC can generate tens of trigger signals for various accelerator components.

The serial data stream from the master AMC also sends supplemental information for the next trigger, such as a trigger number and event data, just after each trigger code. Each entry of the event data consists of an event code and a common delay. The event code is assigned to each output channel of a slave module, and if the received event data has the event code of the channel, a trigger signal is emitted from the channel. The delay of the trigger timing from the master trigger is the sum of the common delay from the master and the local delay set to the slave channel. A 24-bit counter is used for the delay generation and the maximum delay time is 33 ms for a 509 MHz case.

The trigger output rate for each event can be the same as the master trigger rate and it can be reduced to $1/n$ by sending an event code for every n triggers. Four tables that define the trigger pattern are prepared with a maximum length of 64 shots. This length is enough to cover how to generate the triggers for more than one second. We can generate arbitrary patterns by updating the contents and switching the table index every second or so.

The trigger module is also equipped with some frequency dividers of the acceleration rf signal. These frequency-divided signals can be output from any specified channel. Some asynchronous triggers at any timing can also be delivered to all the slave AMCs for data taking for postmortem analysis at an alarm signal from an accelerator component.

Trigger AMC

We designed the hardware of the trigger AMC to realize the trigger distribution functions described above. The block diagram of the trigger AMC is illustrated in Fig. 2. Trigger signals are processed by a field-programmable gate array (FPGA), Xilinx XC7K325T.

This AMC has 5 Small Form-factor Pluggable (SFP) optical transceivers on the front panel and they are connected to high-speed serial ports on FPGA (so-called GTX). One is to receive the optical trigger signal and the others are to fan out the signal. A high-density connector of VHDCI-68 is mounted on the front panel and 32 low-voltage differential signals (LVDS) are integrated (16 inputs and 16 outputs). Since the AMC backplane has 8 pairs of bus lines (TX/RX 17-20) shared by all the AMC slots, multipoint LVDS (M-LVDS) transceivers are used for these lines to receive or transmit trigger signals. A 4-lane PCI express, 5 GTX links, and module management controller (MMC) lines are also connected to the AMC backplane for communication with a CPU and other modules. The Zone 3 connector is also utilized to distribute trigger signals: 16 inputs, 16 outputs, and 2 GTX links. These I/Os can be used by a Rear Transition Module (RTM) to distribute more trigger signals from the rear side.

The clock signal for the FPGA can be selected from the front panel, Zone 3, AMC backplane (TCLK), and an internal oscillator. Both 509 MHz and 238 MHz can be applied to the external clock input. The FPGA itself is driven by the clock frequency of around 250 MHz (509 MHz / 2 or 238 MHz) and the trigger signal can be generated by both rising and falling edges. Therefore, the delay precision is approximately 2 ns with this clock. To adjust the timing more precisely, the tap delay function of the FPGA is also implemented. The resolution of the tap delay is approximately 80 ps and the number of maximum taps is 32 (~2.5 ns maximum). Therefore, we can adjust the timing with ~80 ps resolution within the ~2 ns period.

Level Converter

For the interface between the trigger AMC and various accelerator components, we also developed a trigger level converter. The block diagram of the level converter is shown in Fig. 3. The level converter has an FPGA, Xilinx XC7S50, that is connected to VHDCI-68, LEMO, and SMA connectors on the front panel, and M12 X-coded connectors on the rear panel. The logic level of the VHDCI-68 is LVDS and the number of I/Os is 16 inputs and 16 outputs. The LEMO connectors are driven by low-voltage transistor-transistor-logic (LVTTL) transceivers and there are 8 inputs and 16 outputs. The SMA connectors are driven by 50 Ω LVTTL buffers and the number of outputs is 8. The rear panel has 8 M12 X-coded connectors that are driven

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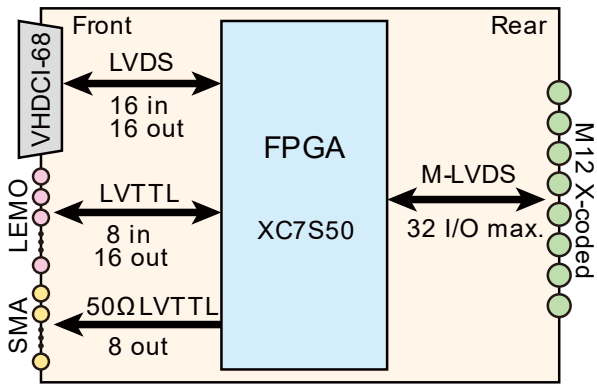

Figure 3: Block diagram of the level converter.

by M-LVDS transceivers. LVDS signals from the M12 connectors are suitable for relatively long transmission lines and noisy environments. The signal transmission network among the I/O connectors can be freely configured by the FPGA firmware.

PERFORMANCE

Trigger Distribution Function

We confirmed all the trigger distribution functions implemented in the trigger AMC. The optical link between the AMCs was appropriately established and the master trigger signal and the event data were distributed to all the slave AMCs. The trigger output timing was precisely delayed from the master trigger timing for a given delay. The trigger output pattern for each channel was also confirmed to be correct as configured to the event table on the master AMC and to the local setting on the slave AMC. An asynchronous trigger was also distributed appropriately and a frequency-divided clock output was generated correctly.

Timing Jitter

Timing jitter between the trigger outputs of master and slave AMCs was evaluated. The master and slave AMCs are connected by an optical fiber and their trigger outputs are observed by a high-speed oscilloscope. The clock frequency was 238 MHz and both the master and slave AMCs are driven by the external clock. A 10 Hz master trigger signal was generated by a pulse generator and fed into the trigger AMC.

The result from the jitter measurement is shown in Fig. 4. The timing jitter between the two trigger outputs from master and slave AMCs was 42.5 ps std. and that between the clock signal and the master AMC output was 40.1 ps std. These jitters are significantly smaller than the clock period and sufficient for most accelerator applications. Some timing-critical components may require one order of magnitude better jitter performance than this result. Even in this case, although a high-speed flip-flop is needed for retiming the trigger signal with the reference clock, enough jitter performance can be realized by additional electronics.

Reliability for Long term Operation

This timing system has been in use at the NewSUBARU since Feb. 2021. One master trigger AMC and four slave AMCs are used. The system had no serious failure for more than one-year operation.

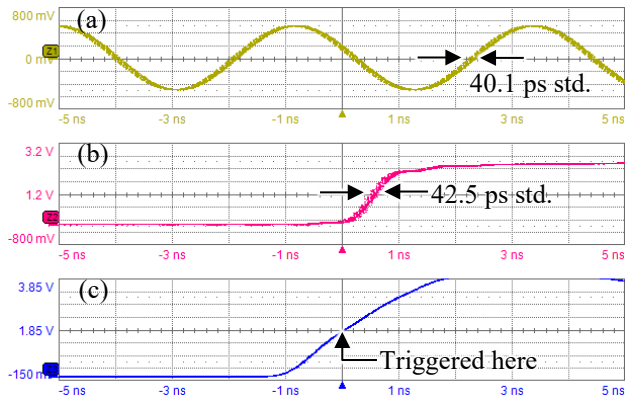

Figure 4: Oscilloscope waveforms from the timing jitter measurement. The external 238 MHz clock is shown in (a), and the trigger outputs from the slave and master AMCs are shown in (b) and (c), respectively. The oscilloscope was triggered by the rising edge of the trigger output from the master AMC (c).

SUMMARY

To synchronize various accelerator components based on MTCA.4, we designed an intelligent and precise trigger distribution system and developed a trigger AMC and a level converter. The trigger signal and supplement information were appropriately delivered by high-speed serial data links through optical fibers. The trigger timing and output pattern were appropriately controlled by using the event data distribution function. The output timing was precisely adjusted by counting the clock of 509 MHz or 238 MHz. The tap delay with ~80 ps step enabled fine-tuning of the output timing within the clock period. Other functions, such as frequency-divided signal output and asynchronous trigger distribution were also implemented. We evaluated the timing jitter of the trigger output and the result was approximately 40 ps std., which is sufficient for most applications. This timing system was installed to SPring-8, SACLA, and NewSUBARU, and various MTCA.4-based electronics are precisely synchronized with each other.

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