ISBN: 978-3-95450-227-1 ISSN: 2673-5490 doi:10.18429/JACoW-IPAC2022-TUPOTK050

DEVELOPMENT OF Zynq SoC-BASED EPICS IOC FOR KOMAC REMOTE CONTROL SYSTEM*

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Abstract

The KOMAC proton accelerator consists of a 100 MeV linear accelerator and beam lines for beam services. Devices of various form factors are used as control systems in accelerator control systems and beam diagnosis systems. With the recent upgrade of the control system, a Zynq-based control system has been developed that enables the latest technology and low cost. The Zynq-based DAQ system was developed by adopting Digilent's Zybo z7 series board and AD7605 analog-to-digital data acquisition system. The Zybo z7 is an embedded software and digital circuit development board built around the Xilinx Zynq-7000 family. The Zynq is based on Xilinx All Programmable System-on-Chip (AP SoC) architecture, which tightly integrates a dual-core ARM Cortex-A9 processor with Xilinx7-series Field Programmable Gate Array (FPGA) logic. The AD7605 is a 4-channel and 16bit ADC with 300 kSPS on all channels. The Zynq SoC-based DAQ system will be used for beam feedback control and RF signal monitoring at KOMAC. This paper introduces the development of configurations for the development of Zynq-based control systems, programmable Logic (PL) builds, and Linux and EPICS porting.

INTRODUCTION

The KOMAC linac and multi-beam lines were designed to provide users with a proton beam under various beam conditions. Representative specifications of the KOMAC linac are maximum beam energy of 100 MeV, and peak beam current of 20 mA, and the adjustable repetition rate is up to 120 Hz. The KOMAC has four beam extraction points at 20 and 10 MeV for proton beam utilization [1].

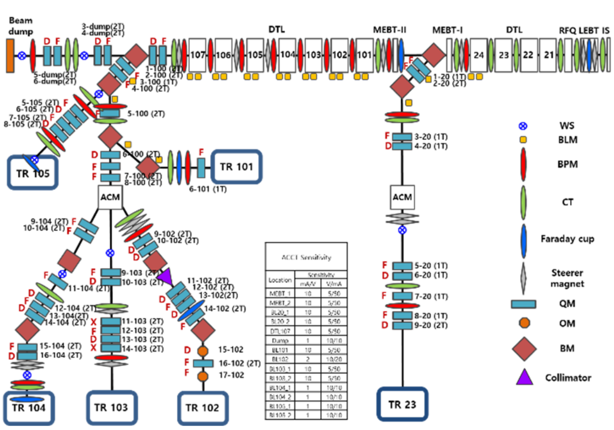

Figure 1: Beam Diagnostic Layout installed on 100 MeV Linac and beam lines.

The accelerated proton beam from the linac is transmitted to the target room via the beam lines. Figure 1 illustrates the beam diagnostic systems located on the Linac and beamlines. Various diagnostic equipment for beam diagnosis are used in linear accelerators and beam lines. The control system processes beam signals from the 100-MeV linac and beam lines and support remote access. Then the beam waveform and beam parameters are visualized in real time. The beam diagnostic equipment in the target compartment was also equipped with a Beam Position Monitor (BPM) and an AC Current Transformer (ACCT). Figure 2 shows the equipment of the radiation testing facilities.

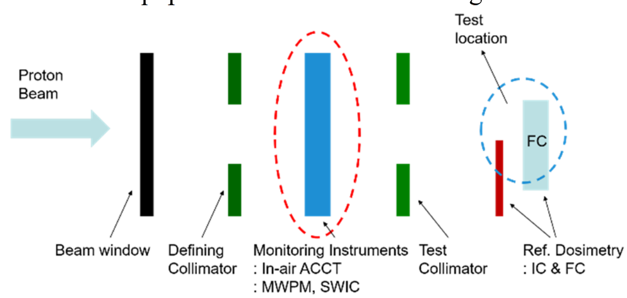

Figure 2: Equipment in radiation impact testing facilities.

When irradiating beams in irradiation test facilities, AC current transformer and faraday cup are used as beam diagnostic equipment to measure beam current. The beam user is required to monitor the accumulated amount of irradiation in real time. The configuration diagram of the system for integrated control of these devices is shown in the Fig. 3 [2].

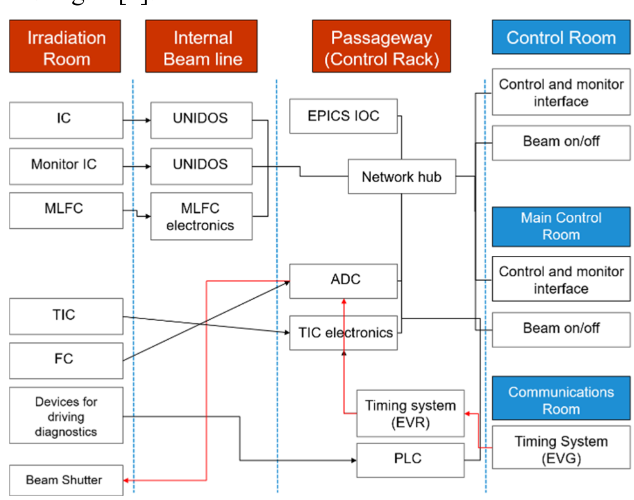

Figure 3: Integrated control interface for target room.

* Work supported through KOMAC operation fund of KAERI by the Korea government (MSIT) (No. 524320-22)
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The beam charge amount is measured and a control system is implemented to measure the beam flux per pulse in real time and block the beam for the accumulated flux. Accordingly, KOMAC decided to develop a new, more efficient control system for beam current measurement and equipment control. In particular, we design and develop a high-performance based data acquisition system using Zynq-7000 [3] architecture platform for high-speed, real-time embedded system-based application design.

DESIGN OF SOC BASED DAQ

The beam width is a maximum of 1ms, so that it has a timing of at least 1.3ms to measure the beam signal. Therefore, when an external trigger signal is generated, the Zynq FPGA records the sampled data in the buffer for 1.3ms. The ADC and Zynq (FPGA) are used to develop a DAQ system for measuring beam current of the Linac and beamlines. It also closes the beam shutter or stops the beam extraction trigger of the KOMAC timing system [4] to block the beam according to the measured result. The requirements of ADC and Zynq are as follows.

- ADC requirements

: 0~10V (input), 300KS/sec sampling
: Input 4 channel / analog output 4 channel
: 1-channel external trigger input (TTL)
: 1-channel trigger output (TTL)

- Zynq requirements

: XC7Z020-2CLG400I with FPGA
: ARM Cortex-A9
: Installing EPICS IOC

- Integrated voltage signal by beam current
- Analog output occurs when input threshold value is exceeded

The Experimental Physics and Industrial Control System (EPICS) middleware used in large accelerators is used for communication and interface of embedded control systems [5]. EPICS IOC is built into Zynq SoC's PS and ADC data processing is implemented in PL. It generates EPICS Process Variables (PV) to provide remote control and monitoring services. The schematic diagram of Zynq and ADC for input/output signals is shown in Fig 4.

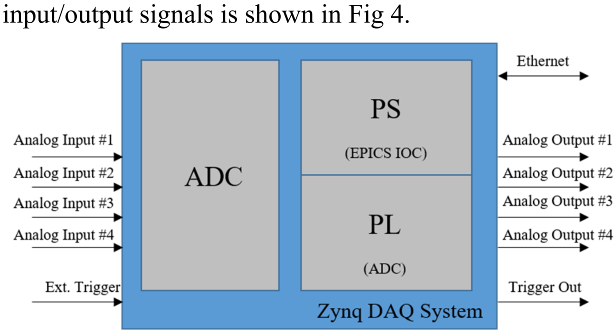

Figure 4: System configuration diagram of Zynq and ADC for input/output signals.

Build DAQ System

Digilent zybo-z7-20 and Analog Device AD7605 ADC [6] were adopted for the development of Zynq SoC-based remote control system. For the development of the ADC device and the Zynq SoC, the development environment was built using the Vivado design suite and the petalinux. Figure 5 shows SoC/FPGA basic design using Vivado and Zynq device.

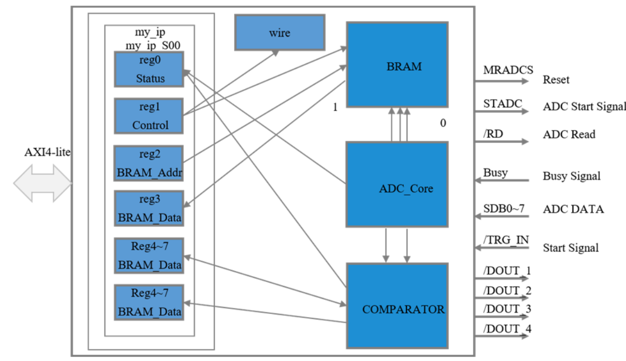

Figure 5: Zynq SoC/FPGA basic design.

The Zynq uses an AXI interface between PS and PL. The PL reads the ADC periodically. When trigger occurs, ADC data is sequentially read and stored in the BRAM. Interrupt occurs when the count of the data stored in the BRAM is the count required (currently 1.3 ms count). The interrupt is input to the PS and delivered to the kernel. When the kernel module catches interrupt, it generates a signal through a specific process of EPICS IOC. When an EPICS IOC receives a signal, it reads the data of the BRAM and generates the waveform data. In order for the kernel module to register the EPICS IOC process, each time the EPICS IOC is started, unload the kernel module and load it anew.

For the architecture design of data acquisition system, AXI peripheral interconnect block is used to interface Zynq processing system with all peripheral interfaces as shown Fig. 6.

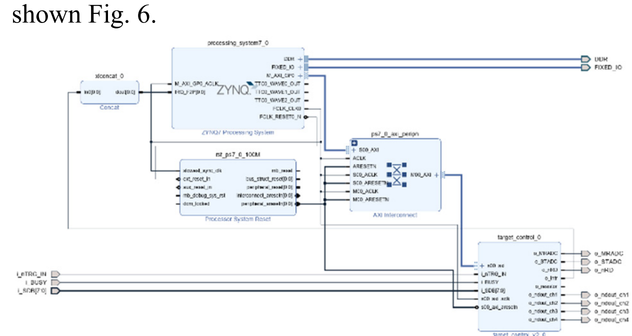

Figure 6: Block diagram of data acquisition system

For IP access, we can check the address connected to the AXI in the Vivado project, and access to the IP is possible through the address. The data is read/write using a pointer connected through memory mapping. If signal is caught in the signal handler function, a function that acquires waveform data is called. The operation of the control system accumulates data by acquiring data from the ADC for a predetermined time and averaging the data for a set time when the external trigger is input. If this accumulated data is greater than a predetermined value, an output signal is generated and a beam shutter is driven. The assembled DAQ system was self-tested as shown in Fig.7, and the performance of Zynq PL and PS was confirmed.

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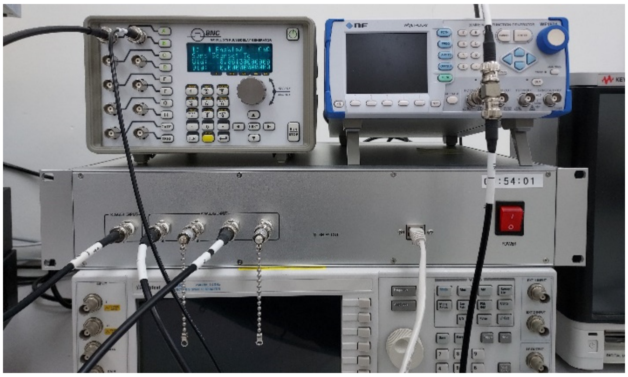

Figure 7: Zynq SoC-based EPICS IOC

EPICS IOC

It uses the petalinux tool to build EPICS on Xilinx Zynq FPGA. After setting up the Xilinx petalinux compiler, cross-compile the EPICS base using the Xilinx cross-compiler. The Petalinux tools offers everything necessary to customize, build and deploy Embedded Linux solution on Xilinx processing systems. We customize the boot loader, linux kernel, linux application. EPICS IOC uses the asynPortDriver of the asyn module to construct the IOC for the Zynq-based DAQ system. When interrupt occurs, a signal is generated in the kernel module, and the signal is caught in the application, and a waveform function is called to obtain waveform data. The waveform function generates data and then calls the callback function. The beam current is array-type data that is allocated to PV of EPICS waveform record, and the waveform data is calculated using waveProce module to calculate statistics of the region of interest. The analog output signal of the DAQ system is used to stop the beam extraction trigger or close the beam shutter after the measured data and the threshold are compared.

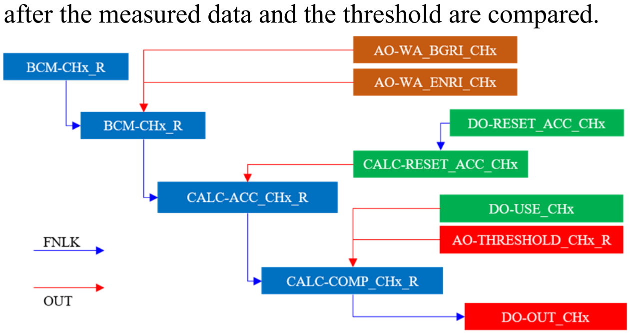

Figure 8: Design of data accumulation and comparison processing using EPICS record

The record design of the EPICS IOC implemented in Zynq PS is shown in Fig. 8. A waveform record for 4 ADC channels is configured and assigned to a waveAnl record for data statistics. The statistically processed value is accumulated in the Calc record and compared with the threshold value in the Calcout record. The analog out signal of the DAQ system is output using a DO record satisfying the condition. Figure 9 shows the CSS top view for beam current monitoring.

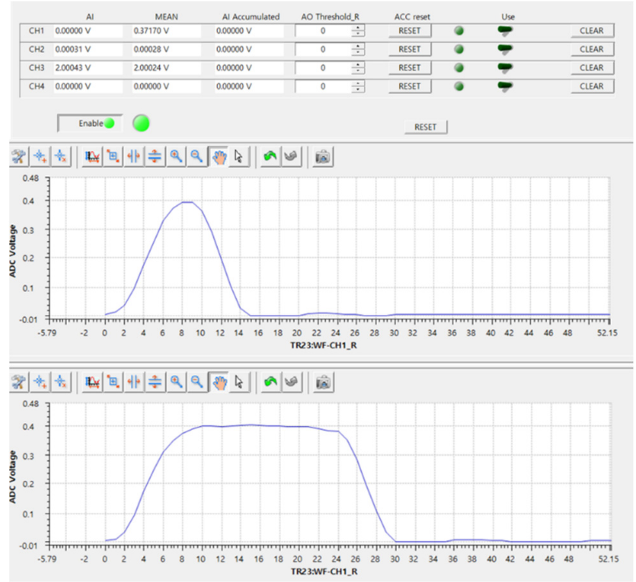

Figure 9: CSS top view for beam current monitoring

CONCLUSION

We decided to develop a new and more efficient control system for beam current measurement and equipment control. We designed and developed a low-cost, high-performance based data acquisition system using Zynq-7000 architecture platform for a real-time embedded system. The control system using a single chip can measure the beam current in the KOMAC Linac and beamlines, and it was verified that it can be used as a control signal to control the timing output trigger to extract the proton beam or to close the beam shutter. Based on the stability of the evaluation board, it is planning to develop it as a single system using Zynq chips.

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