EVALUATION OF FAST ADCS FOR DIRECT SAMPLING RF FIELD DETECTION FOR THE EUROPEAN XFEL AND ILC

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Abstract

For the LLRF system of superconducting Linacs, precision measurements of the RF phase and amplitude are critical for the achievable field stability. In this paper, a fast ADC (ADS5474) was employed to measure the 1.3 GHz RF signal directly without frequency down conversion. In the laboratory, the Signal to Noise Ratio (SNR) of the ADC was studied for different RF input levels, and the temperature sensitivity of the ADC has been determined. A full bandwidth phase jitter of 0.2 degree (RMS) and amplitude jitter of 0.2% (RMS) was measured. For field control of superconducting cavities with a closed loop bandwidth up to 50 kHz, one can expect to achieve a phase stability close to 0.01 degree. The main limitation will be the jitter of the external clock. We represent measurements of the cavity fields at FLASH and compare the result with the existing system with down converter.

INTRODUCTION

The superconducting Linacs in facilities such as European XFEL and ILC, require significant RF field stability up to 0.01 degree in phase and 0.02% in amplitude [1], which are guaranteed by the LLRF system. Precision measurements of the RF phase and amplitude are critical for the achievable field stability for the LLRF system.

Most of the superconducting cavities of European XFEL and ILC work on the frequency of 1.3 GHz, which until recently could not be directly measured by commercially available ADCs. The most widely used way for measurement is to convert the 1.3 GHz RF signal to an intermediate frequency and then sample by ADCs.

Though ADCs with a bandwidth of a few GHz are available since a few years, their resolution was limited to 8 or maximum 10 bits. Recently, ADCs with 12 or even 14 bits are available, making it possible to measure the RF signal directly without frequency down conversion. Direct sampling ADC gets rid of the down converter and makes the RF measurement circuit much simpler and smaller, but will be sensitive to the clock jitter. The ADS5474 is an ADC with 14-bit resolution, 400 MSPS and 1.4 GHz bandwidth, which is suitable to sample the 1.3 GHz signal directly with under sampling scheme. This ADC was evaluated both in the laboratory and for the injector RF system at FLASH.

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RF FIELD DETECTION

The ADC sampling frequency (400 MSPS) is much smaller than the RF frequency (1.3 GHz), so under sampling is used, and the RF signal is measured in a higher Nyquist band. In order to derive the phase and amplitude directly from the sampling, the clock frequency should be synchronized with the RF frequency and chosen based on the non-IQ sampling scheme [2]. The possible sampling frequency f_s is

$$f_s = \frac{f_0}{k + \frac{m}{n}}, \quad k = 0,1,2... \tag{1}$$

where f_0 is the RF frequency, m and n represent the phase difference between two adjacent samples

$$\Delta\varphi = \frac{m}{n} \cdot 2\pi \tag{2}$$

The I and Q baseband components can be calculated by the ADC sampling according to the formula below

$$I = \frac{2}{n}\sum_{i=0}^{n-1} x_i \sin(i\Delta\varphi)$$
$$Q = \frac{2}{n}\sum_{i=0}^{n-1} x_i \cos(i\Delta\varphi) \tag{3}$$

where x_i is the ADC sampling data.

The non-IQ demodulation by equation (3) can separate and suppress the harmonics of the carrier frequency.

During testing, the sampling frequency is chosen to be 178.8990825 MHz (m = 4 and n = 15), and the RF frequency is mapped to 47.7064225 MHz.

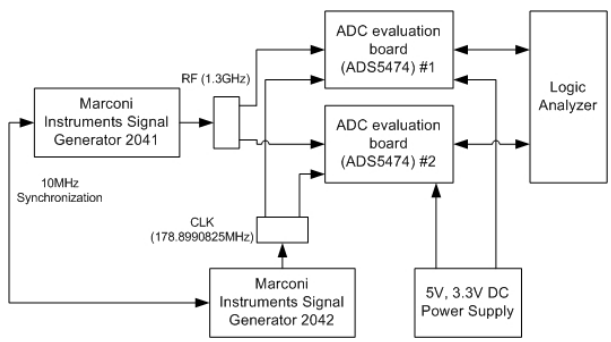

Figure 1: ADC testing stand in laboratory.

NOISE CHARACTERISTICS

The ADC evaluation board is measured in laboratory for estimating the noise characteristics. The testing stand is shown in Fig. 1. Two synchronized low noise signal generators are used for clock and RF signals. The ADC sampling data are recorded by a logic analyzer. The

second ADC evaluation board is installed for the temperature sensitivity measurements for phase and amplitude.

For different RF input power, the SNR and noise floor of the ADC are measured by Fourier transform (see Fig. 2). It is seen from the figure that when the RF input power gets larger, the noise floor becomes larger, but the SNR becomes more constant.

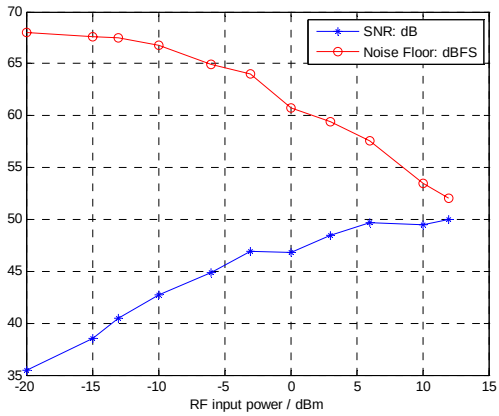

Figure 2: Signal to noise ratio and noise floor of the ADC with different RF input power.

For the direct sampling ADC, when the RF input power is large, the noise will be dominated by the external clock jitter effect. The limitation to SNR based only on clock jitter can be determined by the equation

$$SNR_{jitter} = -20\log_{10}(2\pi f_{RF}\Delta t) \qquad (4)$$

where f_{RF} is the RF frequency and Δt is the RMS clock jitter. For the signal source (Marconi Instruments 2042) used for clock, the typical single sideband (SSB) phase noise is shown in Table 1 [3].

Table 1: SSB Phase Noise of Marconi Instruments 2042

Offset Frequency	SSB Phase Noise (dBc/Hz)
100 Hz	-81
1 kHz	-121
>= 20 kHz	-140

From Table 1, the time jitter of the clock signal is estimated to be 0.3 ps (RMS), which corresponds to a SNR of 52 dB according to equation (4) when the RF frequency is 1.3 GHz. This is the limitation of the SNR with the setup shown in Fig. 1.

The spectrum of the sampled RF signal is shown in Fig.3, with the RF power of 12 dBm, and the SNR of 50.5 dB.

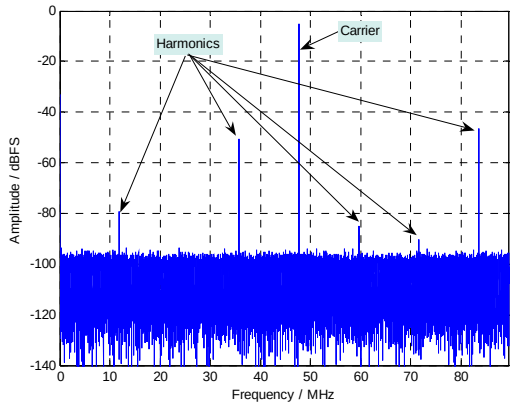

Figure 3: Spectrum of the sampled RF signal.

The phase and amplitude of the RF signal can be derived from equation (3). For the data shown in Fig. 3, the measured phase jitter is about 0.05 degree (RMS) and amplitude jitter 0.06% (RMS), where equation (3) can be viewed as a bandpass filter with a bandwidth of about 10 MHz. With the full Nyquist bandwidth of 89.45 MHz, one can estimate a phase jitter of about 0.2 degree (RMS) and amplitude jitter 0.2% (RMS).

For the LLRF system of European XFEL, the direct sampling ADC can be used for measuring the cavity probe signals, which acts as the input to the feedback loop. The TESLA typed superconducting cavity has a bandwidth of about 200 Hz, so with a feedback gain of 250, the closed loop bandwidth will be about 50 kHz. The ADC noise will be low pass filtered by the feedback loop, so the phase and amplitude jitter will be lowered by the factor of

$$C = \sqrt{\frac{f_{BW,closed\_loop}}{f_{BW,Nyquist}}} = \sqrt{\frac{50kHz}{89.45MHz}} \qquad (5)$$

So, even with the feedback gain high as to 250, one can expect a phase stability of better than 0.01 degree and amplitude stability of better than 0.01%, which can meet the requirements for the main Linac of the European XFEL.

TEMPERATURE STABILITY

The temperature sensitivity of the ADC is important for the long term stability. The phase and amplitude drifts due to the ADC temperature change are measured in the laboratory. The testing stand is shown in Fig. 1; one ADC chip is cooled by cold spray while another ADC is used for measuring the RF signal as phase reference.

The measured phase and amplitude drifts according to the ADC chip surface temperature are shown in Fig. 4. The phase temperature coefficient is 0.14°/°C and the gain temperature coefficient is -0.03 %FS/°C, which are acceptable for the accelerator environment. The phase and amplitude drifts with temperature are quite linear, which can be compensated by measuring the ADC temperature.

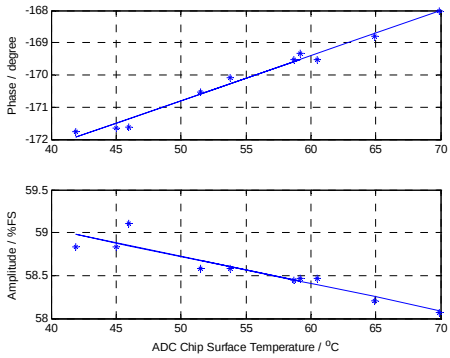

Figure 4: Phase and amplitude drift measurements.

MEASUREMENTS AT FLASH

The ADC boards are evaluated by measuring the probe signals in ACC1 at FLASH. The measurement setup is similar to Fig. 1, except that the RF signals to the ADC boards are replaced by a cavity probe signal and master oscillator signal respectively. Because the clock signal is not synchronized with the FLASH RF, we need a master oscillator signal as reference measured with a second ADC to compensate the phase slope.

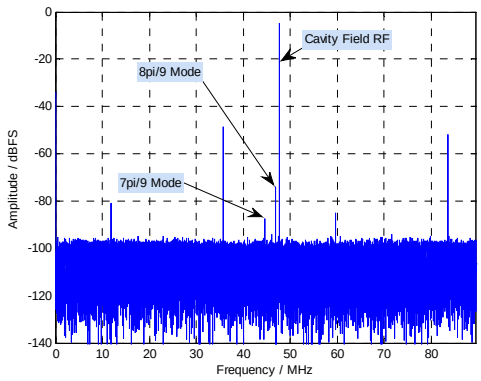

Figure 5: Spectrum of the probe signal of cavity 8 in ACC1.

Fig. 5 shows the spectrum of the probe signal of cavity 8 in ACC1 measured by the ADC. Comparing to Fig. 3, there are two additional frequency components except for the harmonic frequencies, which show the excitation of the $8\pi/9$ and $7\pi/9$ modes of the cavity.

The amplitude and phase of the probe signal of cavity 8 in ACC1 are derived from non-IQ demodulation, see Fig. 6, and the measurements from the monitoring ADCs with down conversion to 250 kHz IF are also shown for comparison.

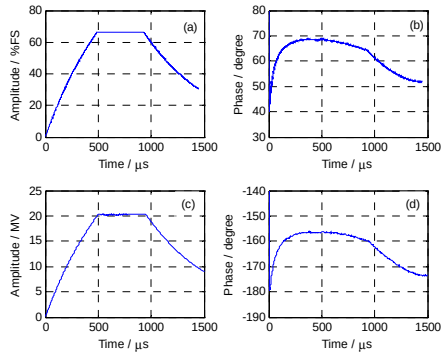

Figure 6: Amplitude and phase measurements. (a),(b): Measured by direct sampling ADC; (c),(d): Measured by monitoring ADC in ACC1 at FLASH.

During the flat top of the RF pulse, the direct sampling ADC exhibits a phase jitter of 0.05 degree and amplitude jitter of 0.054% (with a bandwidth of about 10 MHz); while the monitoring ADC gives a phase jitter of 0.09 degree and amplitude jitter of 0.078% (with a bandwidth of about 500 kHz).

SUMMARY

In this paper, a high bandwidth ADC (ADS5474) was evaluated both in laboratory and FLASH. A full bandwidth phase jitter of 0.2 degree (RMS) and amplitude jitter of 0.2% (RMS) was achieved. The temperature stability of the ADC was also measured and as the results, the sensitivity for the phase is 0.14º/ºC and for the amplitude -0.03 %FS/ºC. During the test at FLASH, the direct sampling ADC demonstrated even better noise characteristics than the existing monitoring ADC.

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