PERFORMANCE OF DIGITAL LOW-LEVEL RF CONTROL SYSTEM WITH FOUR INTERMEDIATE FREQUENCIES

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Abstract

In superconducting accelerators, an FPGA-based low-level RF (LLRF) system is employed with a digital feedback control system to satisfy the stability requirement of the accelerating field. In the digital LLRF systems, an RF signal picked up from a cavity is down-converted into an intermediate frequency (IF) signal to estimate the I and Q components of the RF signal. A new digital LLRF system that uses four different IFs has been developed to decrease the number of analog-to-digital converters (ADC) required during the feedback operation of the RF sources.

In this study, the digital LLRF system with four different frequencies is examined and the feedback operation using a superconducting cavity is performed at the Superconducting RF Test Facility (STF) at KEK. The performance of the digital LLRF system is reported by measuring the stabilities of the accelerating fields.

INTRODUCTION

A single RF system of the International Linear Collider (ILC) consists of three accelerating cryomodules (two of these are composed of nine superconducting cavities each and one is composed of eight cavities) and a klystron that generates RF power [1]. In the ILC, an accelerating field stability of 0.07% in amplitude and 0.24° in phase is required for its operation. In order to meet this requirement, the RF field is controlled with vector-sum feedback (FB) and feedforward (FF) mechanism using a digital low-level RF (LLRF) system based on an FPGA/DSP board.

In the digital LLRF system, the RF signal picked up from a cavity is down-converted into an intermediate frequency (IF) signal while retaining the amplitude and phase information of the RF signal. The IF signals are sampled by analog-to-digital converters (ADCs) with a constant sampling rate (SR) and the amplitude and phase information (or I and Q components) of the RF signal are determined by digital signal processing.

In the case of vector-sum FB control, the number of ADCs required for field detection is equal to the number of cavities, as shown in Figure 1(a). In the case of the ILC, one RF station requires 26 ADCs to operate the RF field with FB control. It is difficult to construct an FPGA board that can hold such a large number of ADCs because the number of lines between the FPGA and the ADCs increases as the number of ADCs increases.

Currently, a digital LLRF control system using a new IF-mixture technique is being developed in order to decrease the number of ADCs required for field detection. In this technique, the RF signals from different cavities are down-converted into different IF signals and these IF signals are then combined using a combiner, as shown in Figure 1(b). The I and Q components of each IF signal are evaluated from the combined IF signal sampled by ADC. By employing two IFs in the digital LLRF system, the number of ADCs can be reduced to half the original value.

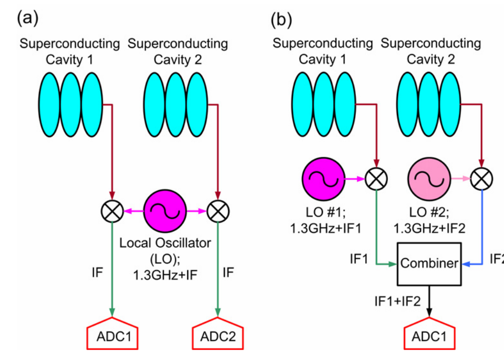

Figure 1: Schematic diagram of the digital LLRF system: a) conventional and (b) IF-mixture technique.

A digital LLRF system employing the IF-mixture technique on two IF signals has been developed and the performance of FB operation has been evaluated by using two cavity simulators [2]. In this study, we developed a digital LLRF system with four IF signals that operated a superconducting cavity [3] at the Superconducting RF Test Facility (STF) at KEK.

IF-MIXTURE TECHNIQUE

The down-converted IF signal is expressed as follows:

$$x(t) = I(t)\cdot\cos(\omega_{IF}t+\varphi) + iQ(t)\cdot\sin(\omega_{IF}t+\varphi)$$

where $I(t)$, $Q(t)$, and φ are the I and Q components and the loop phase of the cavity, respectively, and $\omega_{IF} = 2\pi \cdot IF$. When the sampling rate of the ADC and the frequency of the IF signal satisfy the condition M・*IF* = N・*SR* (N is an integer and M is an integer greater than 3), the I and Q components of the IF signals can be numerically calculated using the following equations for averaging consecutive signal samples [4, 5].

$$I = \frac{2}{M}\sum_{n=1}^{M} x_i(n)\cdot\cos\left(\frac{2\pi\cdot N}{M}\cdot n\right)$$
$$Q = \frac{2}{M}\sum_{n=1}^{M} x_i(n)\cdot\sin\left(\frac{2\pi\cdot N}{M}\cdot n\right) \quad (1)$$

It is expected that the influence of noise and jitter caused by the ADC sampling can be reduced by averaging the signal samples.

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A specific set of I and Q components are evaluated and the remaining I and Q components are cancelled by selecting the appropriate N and M values in the IQ algorithm (1) such that the combined IF signal can be expressed as a combination of frequencies with (N1/M) · *SR*, (N2/M) · *SR*, and so on. In this experiment, we choose 40.625 MHz as the sampling rate of the ADC and as the FPGA clock rate. The combinations of (M, N1, N2, N3, N4) = (9, 1, 2, 3, 4) and (24, 3, 4, 6, 8) are selected to demonstrate the IF-mixture technique using four IFs.

DIGITAL FEEDBACK SYSTEM

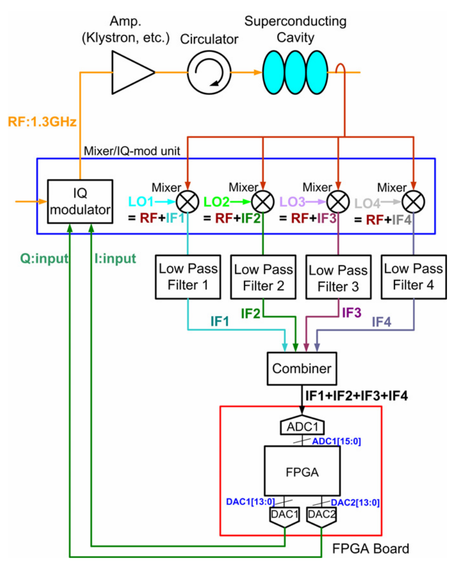

Figure 2: Schematic of system configuration.

The configuration of the digital LLRF system employing the IF-mixture technique consists of an FPGA board, a mixer/IQ-mod unit, and a signal distribution system. The block diagram of the configuration is shown in Figure 2. The FPGA board consists of an FPGA chip (VirtexIIPro30), ten 16-bit ADCs (LTC2204), and two 14-bit DACs (AD9764). This board is installed in a CompactPCI to control the RF field. The mixer/IQ-mod unit consists of ten active mixers (AD8343) and two IQ modulators (AD8349). These units were developed for the STF [6].

The DACs on the FPGA board are connected to the IQ modulator. The RF signal outputted from IQ modulator is amplified by a klystron and is used to drive a cavity. The RF-probe signal from the cavity is divided into four RF signals, and each RF signal is down-converted into the corresponding IFs. These IF signals are filtered by using an appropriate low-pass filter to eliminate the harmonics and then combined using a combiner (Mini-circuits, ZMSC-4-3). The combined IF signal is directly transmitted to the ADC and processed by the FPGA.

Signal Distribution System

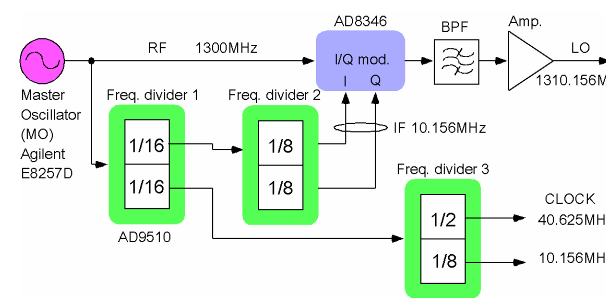

Figure 3: Schematic of signal distribution system.

The signal distribution system consists of a master oscillator (MO, Agilent E8257D), evaluation board containing programmable clock distribution ICs (AD9510/PCB), IQ modulator (AD8346) and a band-pass

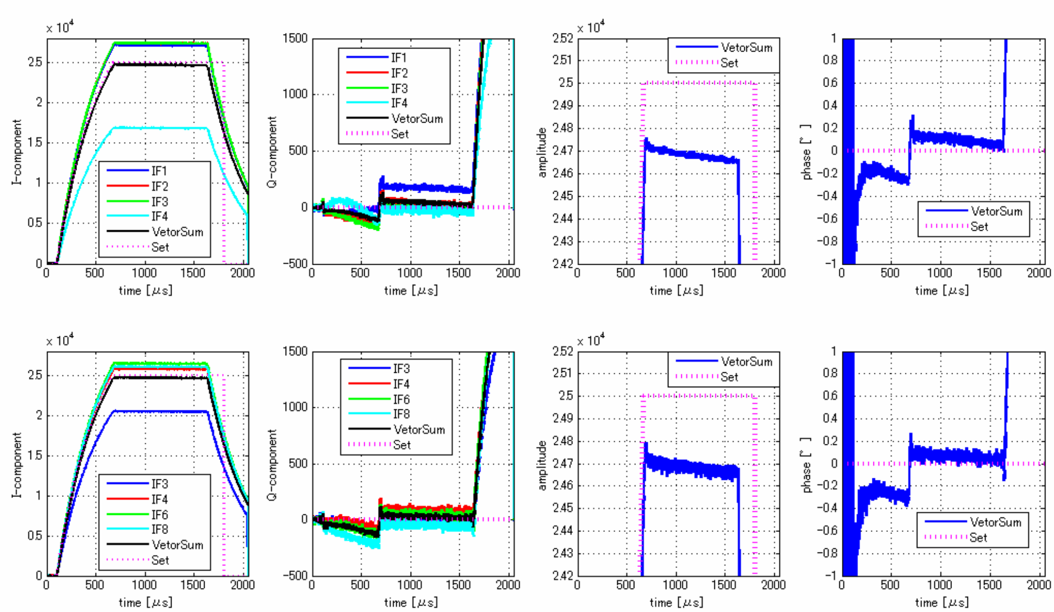

Figure 4: Measured I/Q and amplitude/phase components with FB operation for (M, N1, N2, N3, N4) = (9, 1, 2, 3, 4) and (24, 3, 4, 6, 8).

filter, as shown in Figure 3. This system generates a 40.625 MHz clock signal for the FPGA board along with several different local oscillator (LO) signals; these signals are synchronous with the 1.3 GHz RF signal. The phase noise of each frequency is measured using Agilent E5052A; the root mean square (RMS) phase noises estimated by integration over 10Hz to 10MHz were found to be 0.015° for MO and 0.02° for LO, respectively.

FEEDBACK PERFORMANCE

The feedback performance of this digital LLRF system using the IF-mixture technique is evaluated using a superconducting cavity at the STF at KEK.

Figure 4 shows the result obtained at the set point of 25,000 under P control for a gain of 80 (without FF) in the case of (N, M1, M2, M3, M4) = (9, 1, 2, 3, 4) and (24, 3, 4, 6, 8). As shown in Figure 4, the feedback loop of the system is closed and the I and Q components of the cavity signal are separated from those of the combined IF signal. In both combinations of (M,N1～N4), the corresponding errors in the amplitude and phase observed at the flat top from 750 to 1600 μs are 0.08% (RMS) and 0.03° (RMS), respectively.

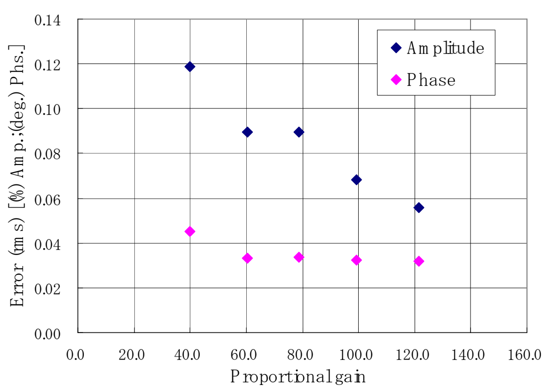

Figure 5: Errors in amplitude and phase at flat top.

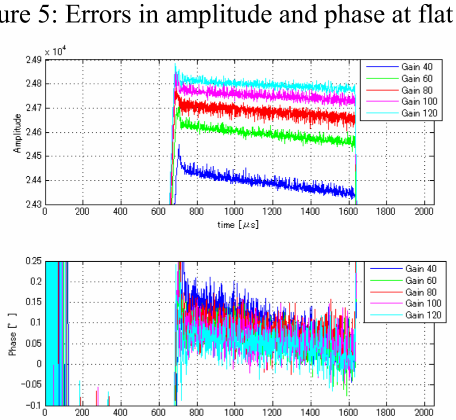

Figure 6: Amplitude and phase at the flat top with different proportional gain.

Figure 5 shows the relation between the proportional gain (P-gain) and the amplitude and phase stabilities at flat top. The P-gain is calculated from the difference between the set point and the average of the measured flat top. The FB operation becomes unstable when the P-gain is greater than 140.

In the region of stable FB operation, the error in the phase is constant at 0.03° (RMS), but the error in the amplitude depends on the P-gain. Figure 6 shows the observed amplitude and phase at the flat top. By adopting an appropriate feed-forward table, the slope in the amplitude at the flat top is expected to disappear. On neglecting the effect of sag, the errors in the amplitude and phase over the period between 1000 μs and 1050 μs, are found to be 0.03% (RMS) and 0.02° (RMS), respectively.

SUMMARY

At the STF, a digital LLRF system employing the IF-mixture technique was operated over a superconducting cavity. In order to demonstrate the IF-mixture technique with the cavity, we developed a signal distribution system that can generate several LO signals. The phase noise of the signals were measured and estimated to be 0.015° (RMS) for MO and 0.02° (RMS) for LO by integration over 10Hz to 10MHz. The FB performance of the system was examined under several P-gains and the stabilities of the amplitude and phase were evaluated. At the flat top, the stabilities of the amplitude and phase were expected to be 0.03% (RMS) and 0.02° (RMS), respectively, by adopting the appropriate feed-forward table.

A cryomodule that installs four superconducting cavities is planned to operate this winter with the demonstration of the digital LLRF system employing the IF-mixture technique.

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