

CSNS LINAC RF SYSTEM DESIGN AND R&D PROGRESS

Jian Li, Xinan Xu, Yuan Yao, Zhencheng Mu, Wenzhong Zhou, Zonghua Zhang, Jimin Qiao,
Institute of High Energy Physics, Beijing, China

Abstract

China Spallation Neutron Source (CSNS) is determined to be constructed in Dongguan, Guangdong province of south China. Now its design and R&D are in progress in IHEP, Beijing. The 324 MHz rf linac is designed with beam energy of 81 MeV and a peak current of 30 mA [1]. In the klystron gallery, five klystron power sources will be used to power the RFQ and the four DTL tanks, and three solid state rf amplifiers will drive two MEBT bunchers and a LRBT debuncher. Now we have already made some progress with some key technologies for linac rf system. The digital low level rf (LLRF) prototype was already developed and successfully applied in beam commissioning of the ADS (Accelerator Driven Sub-critical system) 3.5 MeV RFQ accelerator at peak beam 46 mA, beam duty 7% [1]. A proposed new type of power supply, 100 Hz ac series resonance high voltage power supply, passed acceptance test and a satisfactory test results was obtained. R&D of crowbar and modulator has gotten good performance test data. In this paper, a description of these linac rf R&D activities will be briefly presented.

INTRODUCTION

The rf power systems for CSNS 81 MeV linac operate at rf frequency 324 MHz, repetition rate 25 pps, maximal pulse width 650 μ s, and duty cycle 1.625%. One-rf-unit-per-cavity independent rf control design is adopted. The layout block diagram is schematically shown in Fig. 1. Basic requirements for CSNS klystron rf power source is given in Table 1. There are two klystron candidates to be chosen: TOSHIBA E3740A klystron and CPI 3 MW klystron.

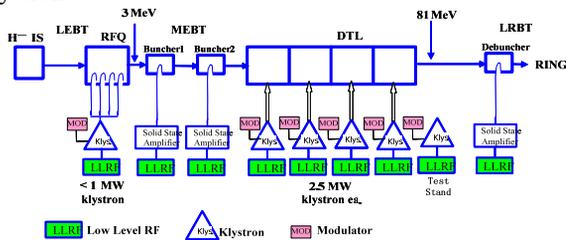


Figure 1: Layout of CSNS linac rf system.

Table 1: Basic Requirements for Klystron RF Power Source

Frequency	324 MHz
Klystron peak output power at saturation	2.5 MW (< 1 MW for RFQ)
Repetition rate	25 pps

Beam voltage pulse width	700 μ s
Rf output power pulse width	650 μ s (Max.)
Efficiency	55% (Min.)
Gain	50 dB (Min.)

DIGITAL LOW LEVEL RF CONTROL

In IHEP ADS project, a 352.2 MHz klystron rf power source provided by CERN was used to drive RFQ accelerator [2]. On this test stand, we carried out R&D of a digital low level rf prototype for CSNS. On October 2007, LLRF prototype passed acceptance test under RFQ beam commissioning. Although the operating frequency of ADS RFQ rf power source is 352.2 MHz, the key technology of this LLRF prototype is the same as that of CSNS, so that it can be easily transplanted into CSNS digital LLRF in the future.

Hardware

A block diagram of LLRF is shown in Fig. 2. An accelerating electric field stability of $\pm 1\%$ in amplitude and ± 1 degree in phase is required. This field control is implemented by a combination of feedback (FB) and feed-forward (FF) algorithms. The two 14bit-ADCs (AD6645) and two 14bit-DACs (AD9764) are installed on FPGA board. The FB PI control and FF control are carried out by one chip of FPGA (STRATIX II series by ALTERA Co.). The DSP (C6000 series by TI Co.) is in charge of communications and translating values between I/Q and Amplitude /Phase. AD8345 chip was adopted as I/Q modulator. The ADS RFQ rf pulse width is 1.4 ms. Because I/Q set tables are both 1024 in length, they are updated every 1.367 μ s during the rf pulse.

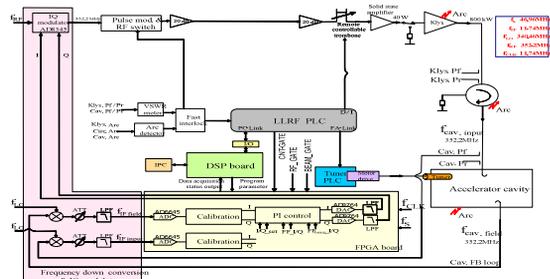


Figure 2: Block diagram of LLRF.

Performance

Under RFQ beam commissioning, the comparison test between without and with FB closed loop control were carried out. In the case of no FB control, As shown in Fig. 3 (a), due to klystron high voltage decline and heavy

beam loading, the amplitude and phase decreased respectively by 9% and 21 degrees in the 1.4 ms pulse. The measured waveforms of no FB control can be seen in Fig. 3 (b): the upper trace is cavity field rf signal, and the lower one is a rf power reflected from RFQ. Beam transmission efficiency is not so high. Once FB control loop closed, the cavity rf field becomes flat. Also, the function of beam FF control was examined. It can effectively improve the transient response of the front and trailing edge of the beam loading. The fluctuations of the amplitude and phase at flattop are stabilized within $\pm 1\%$ and ± 1 degree, respectively (Fig. 4, a). The cavity field waveform is shown in Fig. 4 (b). The RFQ output beam is 48.6 mA and beam transmission efficiency is up to 91.6%. Afterwards, during 48 hours continuous operation test, no problem occurred and the stability was very good.

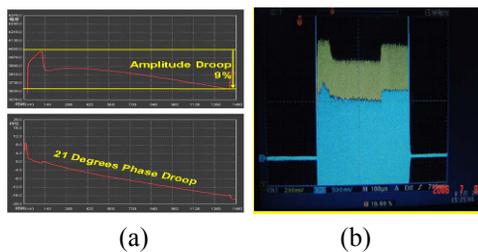


Figure 3: RFQ beam commission without FB control.

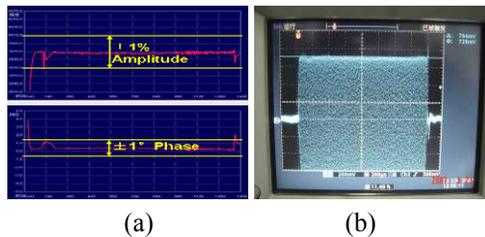


Figure 4: RFQ beam commission with FB and FF control.

AC SERIES RESONANCE HIGH VOLTAGE POWER SUPPLY FOR PULSE KLYSTRON

Design Strategy and Circuit Topology

The schematic diagram of the proposed -120 kV /50 A high voltage power supply for pulse klystron is shown in Fig. 5. Its basic features are AC series-resonant charging and pulse synchronized discharging. It mainly consists of six basic units: IGBT frequency converter power supply, exciting transformer, AC resonant inductance L (1.6 H), AC resonant capacitor C (1.585 μ F), high voltage diodes, DC energy storage capacitor bank Cz. This scheme avoids step-up high voltage transformers and multiphase high voltage rectifiers. The circuit topology is very simple, so it can achieve a good operating reliability and low trip rate, also can be convenient for operation and maintenance. Among these parts, the resonant inductance L and the resonant capacitor C compose a series resonant

circuit, and its natural resonance frequency is $f_0 = 1/(2\pi\sqrt{LC}) = 100$ Hz .

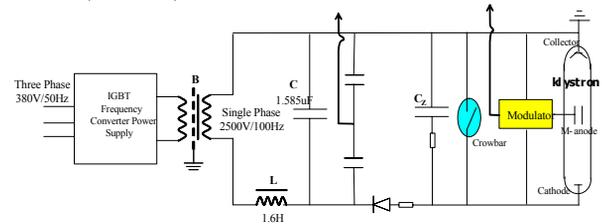


Figure 5: Proposed AC series resonance high voltage power supply for pulse klystron.

By an IGBT frequency converter, the 50 Hz three-phase 380 V power from the mains is converted to f_0 (100 Hz) single-phase power. The exciting transformer step up the low voltage input power to about 2.5 kV /100 Hz. The natural resonance frequency of AC series resonance circuit (L and C) is just 100 Hz. So, because of resonance, 120 kV peak voltage of sinusoid wave on the resonance capacitor C can be obtained. When the AC high voltage wave becomes negative, through high voltage diodes, the DC energy storage capacitor bank Cz can be charged. Meantime, discharging rate of modulator plus klystron is 25 pps, which must be strictly synchronized with AC resonance charging pace. That means, as shown in Fig. 6 (a), every four times the DC energy storage capacitor bank is charged, once discharging pulse occurs. Both of them must be exactly synchronized.

Prototype Performance

Prototype design parameters are: L = 1.6 H, C = 1.585 μ F, circuit unloaded quality factor $Q_0 \geq 250$, required. By computer code simulation in this case, AC to DC efficiency is 87%. On June 2008, the prototype passed acceptance test on ADS klystron power source and the results are quite satisfactory. The measured Q_0 value of inductance is no less than 350. At test condition of klystron cathode voltage 66 kV and output rf power 420 kW, AC to DC conversion efficiency is up to 88%. The performance of the system built agrees with simulation results. In Fig. 6 (a), the sinusoid wave is AC resonance charging voltage on AC resonant capacitor, and the pulse trace is discharging wave of modulator and klystron. Figure 6 (b) shows klystron output rf power. Figure 7 shows AC resonant inductance and AC resonant capacitor.

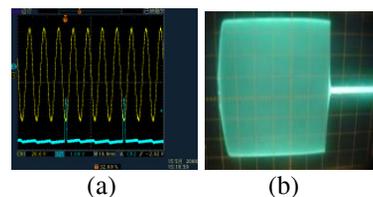


Figure 6: Acceptance test waveforms: (a) AC resonance charging voltage vs. klystron modulation anode voltage (discharging); (b) klystron output rf power.

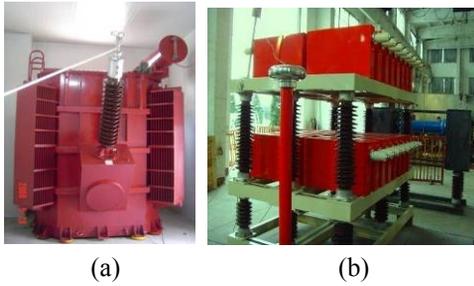


Figure 7: (a) AC resonant inductance; (b) AC resonant capacitor.

Next step, we are going to increase AC resonance frequency up to 400 Hz, so as to reduce noise and volume of the components. The parameters of AC resonance inductance and capacitor are designed as 0.799 H and 0.198 μ F. The newly-designed scheme is ongoing.

MODULATOR AND CROWBAR

M-Anode Modulator

The schematic diagram of modulator is shown in Fig. 8. -110 kV high voltage DC power supply feeds the constant voltage to the klystron cathode. Klystron m-anode pulse voltage is generated by switching the cathode voltage through dividing resistors (R1 and R2) in the m-anode modulator. The anode voltage can be adjusted by the dividing ratio, and the pulse duration is controlled by switching device connected with the resistors in series. The semiconductor switching device is purchased from PEEC company in Japan, the same as that of J-PARC modulator. It mainly consists of 150 FETs (Field Effect Transistor) in series configuration, so that it can withstand -120 kV movement voltage. Unloaded high voltage test (with no klystron load) was carried out at condition of 25 pps / 110 kV / 700 μ s (Fig. 9, a). Its measured rise and fall time are 4.15 μ s and 45 μ s respectively (Fig. 9, b, c).

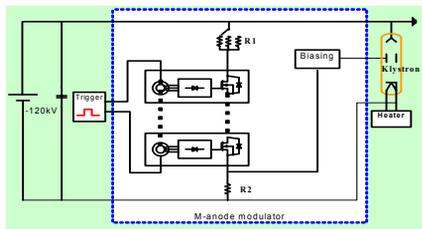


Figure 8: Schematic diagram of m-anode modulator.

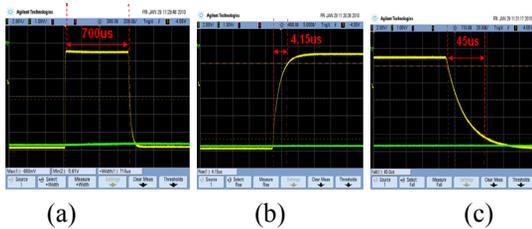


Figure 9: Unloaded high voltage test: (a) 700 μ s m-anode pulse; (b) 4.15 μ s rise time; (c) 45 μ s fall time.

Crowbar

CSNS crowbar prototype is the one of ignitron type. 7703EHVNP ignitron, made by Richardson in USA, serves as crowbar tube. Its peak anode voltage is 50 kV and peak anode current is 100 kA. Therefore, as illustrated in Fig. 10, the 4-series ignitron configuration is adopted. Each ignitron is driven by one sub-trigger module. The control signals of the four sub-modules are fed from a 4-output trigger module via glass optical fibers. We set up a high voltage test stand (Fig. 11, a) to carry out crowbar full voltage -120 kV over current trigger-to-discharging test. The test result shows that the response delay time is 4.5 μ s, less than 6 μ s of design specification (Fig. 11, b).

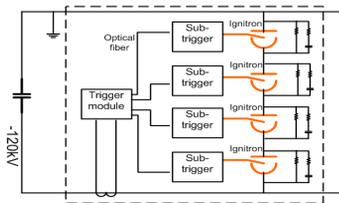


Figure 10: Block diagram of CSNS crowbar.

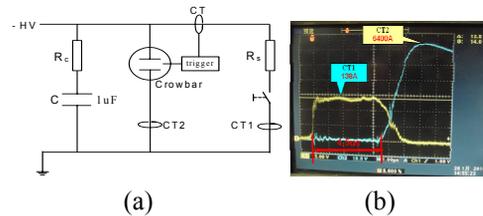


Figure 11: Full voltage -120 kV test: (a) Crowbar test circuit; (b) Delay time from triggering to discharging is 4.5 μ s.

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