COMPACT TIMING SYSTEM WITH FPGA FOR SPRING-8 LINAC

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Abstract

The SPring-8 linac is an injector for the SPring-8 booster synchrotron and the New SUBARU SR ring. The linac emits 1 GeV electron beam to these two rings at 2 Hz by time-sharing. The linac timing system synchronises the electron gun system, the pulsed rf system and the beam diagnosis system etc. It has been assembled with more than one hundred NIM modules and a lot of thin coaxial cables to connect them. To make the timing system small, simple, and reliable, we developed a prototype of compact timing system with FPGA. The developed FPGA includes circuit elements with most of the functions of the NIM modules we are using in the current linac timing system. All of gun trigger circuit in the current system were completely reproduced in it. The timing of the output signal is re-clocked with the master clocks of 500/508 MHz and the rms jitter was less than 1.7 ps. This prototype proved the possibility that the large and complex linac timing system based on NIM modules can be integrated into a small FPGA based timing system.

INTRODUCTION

The timing system of accelerator is usually large and complicated, but the time accuracy around pico seconds is also necessary. To satisfy the time accuracy, the timing systems of traditional accelerators have used NIM signal or NIM modules. But the semiconductor technologies have been advancing these days and very fast and large-scale integrated circuits have been appearing. The FPGA (Field-Programmable Gate Array) is thought to be the most suitable integrated circuit to the timing system of accelerator, because the scale is large enough and it is user-programmable and re-writable. As for the clock speed of FPGA, it was not fast enough five years ago, but the clock speed exceeds 500 MHz now and is likely available for the timing system.

As described later, the timing system of the SPring-8 linac has been also based on NIM modules. It is growing so large and complex for seventeen years' machine operation and improvements that the extension or maintenance of the system is getting difficult. For these reasons, we started to replace the current timing system to a compact timing system with FPGA. The prototype of the compact timing system is described in this paper.

CURRENT LINAC TIMING SYSTEM

SPring-8 is a synchrotron radiation research facility with an 8 GeV storage ring. The SPring-8 linac is an injector for both the SPring-8 booster synchrotron (Sy) and the 1 GeV storage ring New SUBARU (NS). The linac emits 1 GeV electron beam to these two rings at 2 Hz by time-sharing.

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There are three kinds of timing sources, namely, the Sy timing, the NS timing and the Li timing, which were determined according to the selected beam injection route. The Sy timing is used when a beam is emitted to Sy, and the NS timing likewise. The Li timing is used for a solo operation of the linac, when the beam is injected to L2 beam dump or L3 beamline. The Sy timing signals are generated at Sy and then sent to the linac, and the NS timing signals are generated at NS as well. The Li timing triggers are independently generated at the linac.

For each timing source, three kinds of triggers such as the pre-trigger, the gun trigger, and the monitor trigger are prepared in the linac timing system. The pre-trigger is a 2 Hz trigger, distributed to two AWGs (arbitrary wave generators) for generating pulsed reference RF signal [1], an rf pulse modulator, two gun modulators and thirteen klystron modulators. The gun trigger is a continuous 1 Hz trigger, and then is selected out at the injection timing to distribute to the gun pulsers of the two electron guns [2]. The monitor trigger is also a continuous 1 Hz trigger and is distributed to the beam current monitors or the beam position monitors.

The SPring-8 linac timing system has following two special features that complicate the timing system.

1) Time-shared injection

The beam injection to Sy or NS has been time-shared since 2013 for an efficient beam injection called as "fast alternate injection". In the fast alternate injection, all of the Sy timing triggers and the NS timing triggers are switched every 0.5 second [3,4]. It is necessary to synchronize the NS timing trigger to the Sy timing trigger for time-sharing, so that all NS timing sources are generated from the Sy timing pre-trigger.

2) Irregular triggering for energy saving

The 2 Hz modulator trigger to the klystron modulators, which is generated from a pre-trigger, cannot keep the PFN voltage high enough until the discharge time of thyratron, because the PFN voltage decreases during the charging interval of 500 ms in case of 2Hz modulator trigger. For this reason, irregular 4 Hz trigger is used, where another discharge timing was added at 100 ms before the 2Hz modulator trigger for the pre-discharge of the decreasing charge stored in the PFN capacitors [3].

To complete these requirements, many kinds of NIM modules have been used, for example, fanout, AND/OR logic, majority logic, selector switch, delay/gate generator, and precise long delay using 30 bits counter. The number of NIM modules we are using is 161 and the number of NIM bin is 22 at this moment. They are so many that it is not easy to modify the circuit further more and maintain the line connections or validity of the circuit. For these reasons, we decided to develop a new compact linac timing system.

COMPACT TIMING SYSTEM

We adopted the FPGA as a key device for a compact timing system. Recent models have more than 100,000 logic cells and their clock speed exceeds 500 MHz, which satisfy our requirements. We developed a prototype of compact timing system with an FPGA assembled in a 5U rack-mount enclosure. The photograph of the prototype is shown in Fig.1. In the developments, (1) Most of the functions used in the existing NIM module-based system should be included in the prototype, (2) All the gun trigger circuits in the current timing system should be completely programmed in the FPGA.

To keep the compatibility with the current NIM module-based system, the NIM signal standard was decided as the I/O signal of the prototype. Fifty NIM inputs, fifty NIM outputs, three external clock inputs and a display control are on the front panel.

Figure 1: Photograph of the prototype of the compact timing system.

The configuration of the prototype is shown in Fig.2. It is divided mainly into three parts, namely, an I/Q modulation board, an interface board and a FPGA board.

The I/Q modulation board is used to change the phase of the three clocks to give a proper phase. Three RF signals such as Sy 508 MHz (synchronous), NS 500 MHz (synchronous), and Li 500 MHz (asynchronous) are input as external clocks. These clock signals are sent to a 4 x 4 multiplexer on the interface board and then are switched pulse by pulse to fit the input sources.

The interface board converts a NIM input signal to an LVDS signal and an LVDS signal to a NIM output signal because the FPGA cannot handle the NIM signal. We used ADCMP582 ultrafast SiGe PECL output comparators as NIM/LVDS converter. The input signals converted with ADCMP582 are transmitted to the FPGA via FMC interfaces. All of output signals from the FPGA are re-clocked with one of external clock signals to reduce the timing jitter. THS3202DGN 2GHz operational amplifiers were used in the LVDS/NIM converter circuit.

The main FPGA board is an ML623 characterization kit [5] distributed by Xilinx inc., supporting FPGA Vertex 6 (XC6VLX240T-2FFG1156C). The ML623 enabled us to use Vertex6 without producing a new circuit board. Circuit elements corresponding to individual NIM modules were described with a programing language VHDL. Total circuit was programmed on a circuit diagram by connecting the circuit elements. We used ISE Design Suite by Xilinx as a tool for drawing the circuit diagram. Using the circuit diagram, we can easily check and modify the connection of the elements in the circuit.

The Vertex6 features 600 MHz clock speed, 241,152 logic cells, 400 maximum I/Os (in the case of XC6VLX240T). These specifications should be necessary if the current timing system completely shifts to a compact timing system. In the developed prototype, the gun trigger circuit was completely programmed in the Vertex 6. The circuit diagram of the gun trigger circuit is shown in Fig.3. There are three kinds of trigger and clock for the Sy, NS and Li beam route. The downstream after a 6-ch switch in the FPGA is operated with the 4th clock, which is selected out of the three clocks.

For the Sy/NS fast alternate injection, the Sy gun trigger and the NS gun trigger are gated at 1 Hz and then combined at the OR logic. The output of the OR logic is send to the 5th channel of the 6-ch switch and is used as the gun trigger for the Sy/NS fast alternate injection.

The Li trigger is generated from the 60 Hz trigger signal synchronized with the commercial power line. After two dividers, we get the 1 Hz trigger synchronized with the commercial power line.
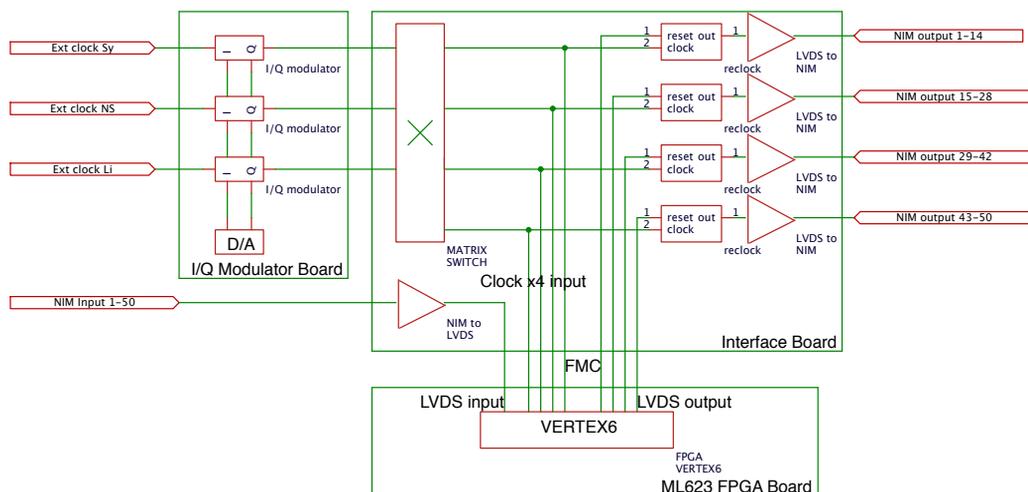

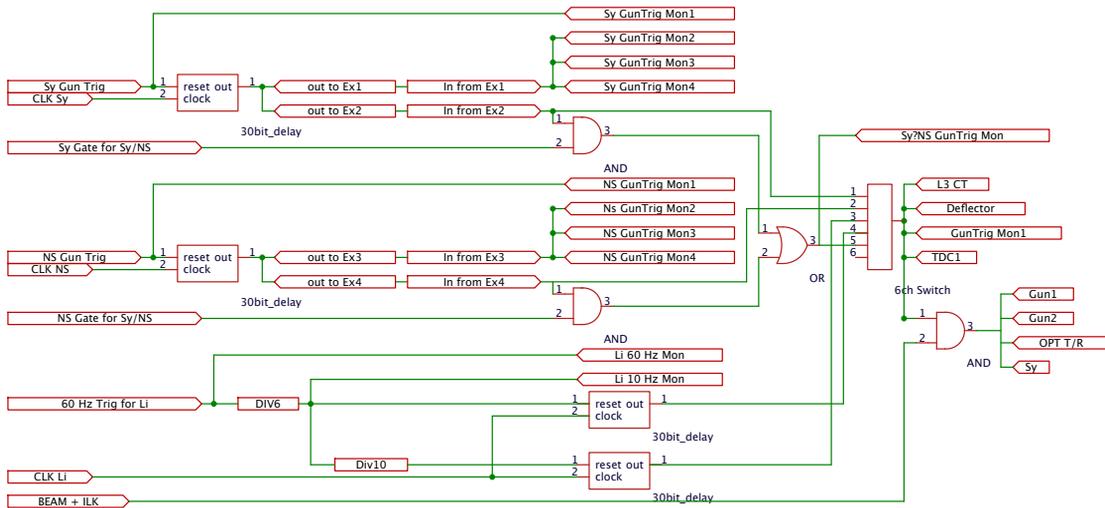Figure 2: Schematic diagram for a prototype of compact linac timing system.

Figure 3: Circuit diagram of the gun trigger circuit to be uploaded to the VERTEX6.

We programmed four 30 bits counter delays in the FPGA. They are required to generate precise timing after a long delay more than 2 ms. The four counter delays are working well at 508 MHz clock speed of Sy. But it was found that adding counter delays more than five make them unstable at some specific delay counts. Because we use totally seventeen counter delays in the current linac timing system, if we fully switch the current system to a compact system, we need some solution to the problem.

JITTER MEASUREMENTS

The timing jitter of output pulse was measured with a Tektronix sampling oscilloscope TDS8200 and 80E03. The output pulse was input to the trigger input of the oscilloscope and the clock signal was input to the CH1 input of 80E03. Measurement result is shown in Fig.4.
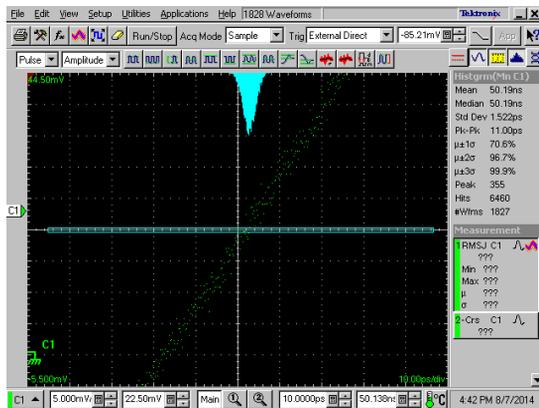

Figure 4: Jitter measurement of the output gun trigger. The rms jitter of the output trigger was 1.5 ps.

The rms jitter measured here was 1.5 ps and all the jitter from other outputs was less than 1.7 ps. In case of the Sy/NS fast alternate injection, the output trigger was also correctly re-clocked by the selected clock signal according to the trigger source. This rms jitter is sufficiently low to operate the linac with a stable acceleration. What is more important is that any meta-stable state in the FPGA did not appear in the system.

CONCLUSION

A prototype of the compact linac timing system with FPGA was developed and tested. The gun trigger timing circuit was fully programed in the FPGA and the circuit worked sucessfully. This prototype proved that the possibility that a large and complicated linac timing system based on NIM modules can be integrated into a small FPGA-based timing system. But the limit of the counter delay operated at 508 MHz was observed and further improvement was found to be necessary if the number of the delay circuit is greater than five. According to the result of the development, we are going to re-write the FPGA program for the pre-trigger circuit and install it in the running linac timimg system in 2015 at the first stage.

ACKNOWLEDGMENT

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