ARCHITECTURE DESIGN FOR THE SwissFEL LLRF SYSTEM

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Abstract

The SwissFEL under construction at the Paul Scherrer Institut (PSI) requires high quality electron beams to generate X-ray Free Electron Laser (FEL) for various experiments. The Low Level Radio Frequency (LLRF) system is used to control the klystrons to provide highly stable RF field in cavities for beam acceleration. There are more than 30 RF stations in the SwissFEL accelerator with different frequencies (S-band, C-band and X-band) and different types of cavities (normal conducting standing wave cavities or traveling wave structures). Each RF station will be controlled by a LLRF node and all RF stations will be connected to the real-time network in the scope of the global beam based feedback system. High level applications and automation procedures will be defined to facilitate the operation of the RF systems. In order to handle the complexity of the LLRF system, the system architecture is carefully designed considering the external interfaces, functions and performance requirements to the LLRF system. The architecture design of the LLRF system will be described in this paper with the focus on the fast networks, digital hardware, firmware and software.

INTRODUCTION

The layout of SwissFEL is depicted in Figure 1 [1]. The accelerator of SwissFEL consists of an S-band RF Gun, two S-band Booster sections, an X-band RF station and 3 C-band accelerator sections. To achieve the high beam stability, the RF jitters with respect to the electron beam for different RF stations should be within the tolerances listed in Table 1 [2].

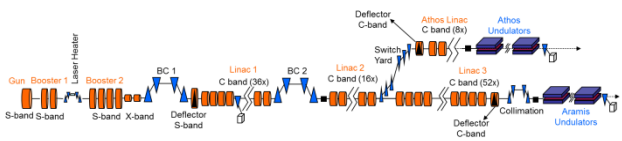

Figure 1: Layout of SwissFEL.

Table 1: RF Stability Requirements for SwissFEL

RF Station	Phase Tolerance	Voltage Tolerance
S-band	0.018 degS	0.018 %
C-band	0.036 degC	0.018 %
X-band	0.072 degX	0.018 %

The LLRF system is introduced to control all the RF stations to provide low noise RF phase and amplitude actuations and precise RF signal detections. Pulse-to-pulse feedbacks will be applied on amplitude and phase at up to 100 Hz (designed repetition rate of the SwissFEL RF system) to achieve the RF stabilities. Drift calibration is required on critical RF signals used for feedback to improve the long-term stability of the system. Automation tools are also required to help the operators to easily setup and operate the RF stations.

VIRTUAL RF STATION

From the view point of the beam physicists, some RF stations can be modelled as a Virtual RF (VRF) station and the output of it is presented by the vector sum of the individual RF stations. The VRF stations with multiple RF stations are listed in Table 2.

Table 2: VRF Stations with Multiple RF Stations

VRF Station	Comment
VRF Booster 1	With 2 S-band RF stations
VRF Booster 2	With 2 S-band RF stations
VRF Linac 1	With 9 C-band RF stations
VRF Linac 2	With 4 C-band RF stations
VRF Linac 3	With 13 C-band RF stations
VRF Athos	With 2 C-band RF stations

The physics applications for beam energy change or beam based feedback will adjust the vector sum amplitude and phase of the VRF stations via the VRF station controllers provided by the LLRF system. The VRF station controllers then determine the amplitude and phase of individual RF stations according to the predefined optimization algorithms. The VRF station controllers will also compensate the failed RF station by increasing the output powers of other RF stations in the same section if possible.

Four control nodes will be defined as VRF station controllers along the accelerator of SwissFEL (see Figure 2). Optical fiber links will be used to interconnect the beam based feedback controller, the VRF station controllers and the individual RF station controllers to support pulse-to-pulse controls, while the Ethernet network with Channel Access protocol will be used as redundancy to improve the robustness of the communications.

HARDWARE ARCHITECTURE DESIGN

The architecture of the LLRF hardware for an individual RF station control is depicted in Figure 3.

The VME based digital hardware is selected because it is well supported by the PSI Control Systems Section. A general carrier board, IFC1210 [3], with a Xilinx Virtex-6 FPGA, a dual-core PowerPC CPU and two HPC FMC slots is used as the general computation platform. The FMC board ADC3110 [4] with 8 AC coupled 250MSPS 16-bit ADC channels is used as the IF digitizer, and DAC3113 with 2 250MSPS 16-bit DAC channels is used

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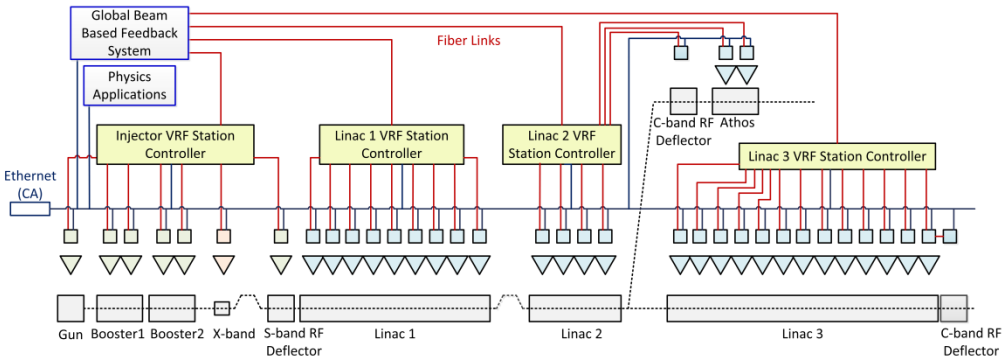

Figure 2: Virtual RF station controllers and LLRF networks.

as the baseband driver for the direct up-conversion vector modulator. The DAC3113 board also has two DC coupled ADC channels to sample the klystron voltage and current signals. The boards are shown in Figure 4.

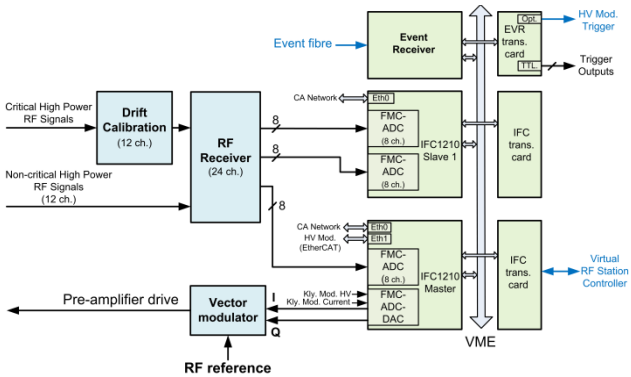

Figure 3: Architecture of LLRF hardware.

For an individual RF station control, two IFC1210 carrier boards will be used with 3 ADC3110 boards providing up to 24 fast ADC channels and a DAC3113 board.

Figure 4: The IFC1210 (left), ADC3110 (right top) and DAC3113 (right bottom) boards.

The usage of the general carrier board and COTS FMC boards results in a modular design with highly reusable firmware and software. Attaching the ADCs and DACs directly with the FPGA also enables fast feedback controls with the latency smaller than 1µs.

The same carrier board will be also used for the VRF station controller design with a different COTS FMC board to provide optical fiber link interfaces to communicate with the IFC1210 Master boards in the individual RF station control nodes (see Figure 3).

The analog hardware for RF signal down conversion, up-conversion, LO and sampling clock generation and drift calibration is assembled into three custom chassis (see Figure 3). The custom chassis provide better shielding, channel-to-channel isolation and cooling due to the relaxed limitations on the PCB size. The design and performance of the C-band prototype analog hardware are described in more details in the contribution [5].

FIRMWARE AND SOFTWARE ARCHITECTURE DESIGN

Overview

The LLRF firmware and software are allocated in the FPGAs and CPUs on the IFC1210 master and slave boards. The overall architecture including the VRF station controller is shown in Figure 5.

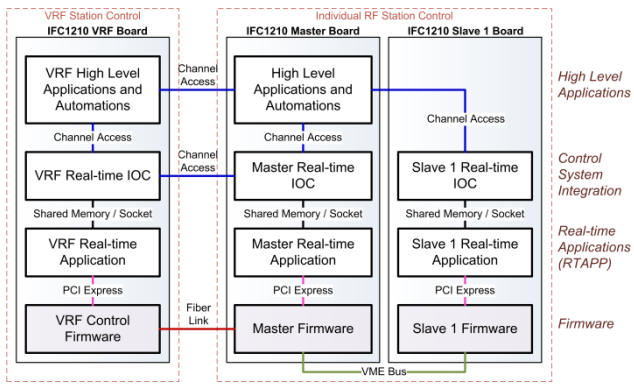

Figure 5: Architecture of LLRF firmware and software.

Firmware

For the individual RF station control, the firmware is used to sample the IF signal outputs from the down converters, demodulate them into I and Q, perform drift calibration and some other processing like vector rotation, filtering and converting to amplitude and phase (see Figure 6). The firmware in the master board also generates RF pulses with the DACs driving the vector modulator.

The VRF control firmware accepts the settings from the beam based feedback system, performs necessary calculations and then adjusts the phase or amplitude of the

ISBN 978-3-95450-142-7

individual RF stations. The communications will be done via fiber links with custom defined protocols.

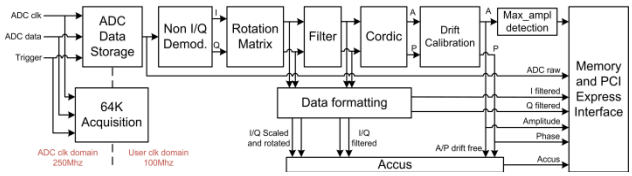

Figure 6: RF signal processing in LLRF firmware.

Real-time Software

The real-time software consists of a standalone Linux application (RTAPP) and an EPICS soft IOC process associated with each other through a shared memory (see Figure 7). Both of them support 100 Hz operation.

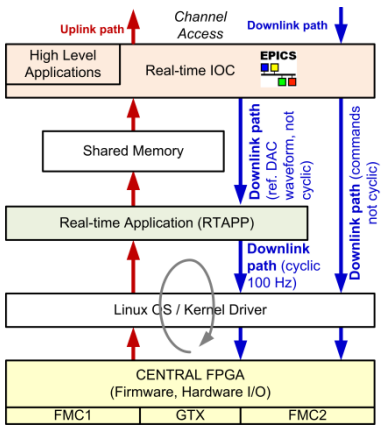

Figure 7: Real-time software and data flows.

When the RF signal processing and data acquisition in firmware are finished, an interrupt will be send to the RTAPP which then reads all the data via DMA. The data of the RF signals are further processed in the RTAPP, like to calculate the average, pulse-to-pulse and intra-pulse jitters of the amplitude and phase, and then saved to the shared memory. Then the RTAPP sends a Linux signal to the IOC to trigger the record processing which posts the data in the shared memory as EPICS Process Variables (PV). The PV processing will update the EPICS CA clients like the GUI and send the data to the archiver.

Pulse-to-pulse feedbacks are implemented in the RTAPP on the master board which directly update the waveforms or the vector rotation parameters for the DAC output in the firmware.

Setting up the firmware registers and buffers can be done synchronously or asynchronously. The synchronous settings can be updated for each RF pulse which is done via the RTAPP. And the asynchronous settings are directly updated by the EPICS record processing via the services provided by the Linux kernel driver for the IFC1210 board.

High Level Applications and Automations

Each RF station has tens of parameters to be set for proper operations. Some high level applications are needed to help the users to determine and setup these parameters. Software tools will be provided to perform the jobs to

- Optimize the parameters like the DAC reference tables for desired RF pulse shape and the DAC offsets to reduce the RF power leakage from the vector modulator.
- Calibrate the coefficients for RF power, vector sum, accelerating gradient and beam phase calculation.
- Identify the parameters like the cavity detuning, vector modulator imbalances and klystron non-linearity.
- Diagnose the system status.

An automation Finite State Machine (FSM) will be created to automate the settings of the entire RF station (see Figure 8).

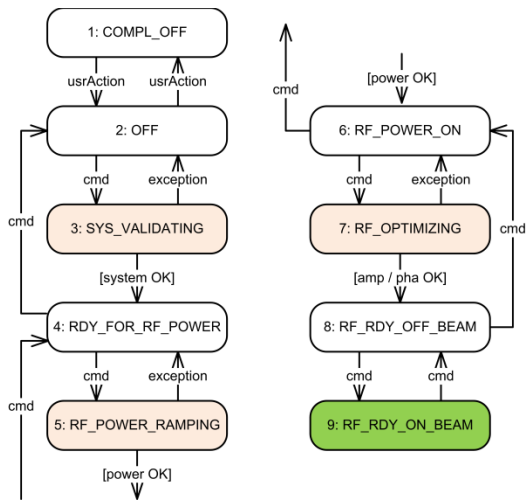

Figure 8: FSM for RF station automation.

CONCLUSION

The architecture of the SwissFEL LLRF system was carefully designed based on the system requirements and the available state-of-the-art hardware and software platforms. It provides good modularity, maintainability, extendibility and reusability. The prototype of the LLRF system has been installed on the C-band RF test stand for SwissFEL. It was well integrated in the control system and provided good support for 100 Hz operation of the klystron including the pulse-to-pulse waveform data acquisition. It was proved to have good robustness for long term operation and has been providing good support to the testing of the high power RF components.

REFERENCES

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