SwissFEL C-BAND LLRF PROTOTYPE SYSTEM

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Abstract

The SwissFEL is driven by more than 30 RF stations at different frequencies (S-, C-, X-band). To control the RF a new, in-house developed digital Low Level RF (LLRF) system measures up to 24 RF signals per station and performs a pulse-to-pulse feedback at a repetition rate of 100 Hz. The RF signals are down-converted to a common intermediate frequency. The state-of-the-art digital processing units are integrated into the PSI's EPICS controls environment. Emphasis has been put on modularity of the system to provide a well-defined path for upgrades. Thus the RF front-ends are separated from the digital processing units with their FMC standard interfaces for ADCs and DACs. A first prototype of the LLRF system consisting of the digital back-end together with a C-band RF front-end was installed in the SwissFEL C-band test facility.

In this report the performance of the prototype system has been compared with the LLRF system requirements for SwissFEL. The critical parameters are high intra-pulse phase and amplitude resolutions, good channel-to-channel isolations, very low phase-to-amplitude modulation and a negligible temperature drift.

INTRODUCTION

SwissFEL is a free-electron X-ray source where 5.8 GeV are required for laser wavelengths down to 1 Å. In its baseline design two electron bunch will be accelerated within one RF pulse. The electron bunch length will be 25 fs (rms) and the spacing between them amounts 28 ns [1].

The Low Level Radio Frequency (LLRF) system is designed to control one RF station. Depending on the location along the machine the LLRF system controls the accelerating fields of up to 4 RF structures. The modular system consists of a common digital processing unit and a frequency dependent RF front-end which converts the different RF frequencies to a common intermediate frequency (IF). A first prototype system was developed with an RF front-end at C-band frequency.

Table 1: SwissFEL RF parameters

Parameter	Value
C-band frequency:	5.712 GHz
Repetition rate:	100 Hz
RF pulse length:	0.02 – 5 µs
Amplitude stability:	1.8e-4 rel. (rms)
Phase stability:	0.036 deg (rms)
Channel-to-channel drift:	0.1 deg / day

Figure 1 shows the topology of one C-band RF station where the reference RF signal is modulated by a vector modulator, amplified by one klystron and fed into four C-band accelerating structures. The input signal before and after the structure is measured and a vector sum is calculated which is required for a pulse-to-pulse feedback.

The RF tolerances for a C-band RF station are summarized in Table 1. The phase tolerances can be divided into the individual components by assuming that the jitter contribution is uncorrelated and equally distributed amongst the subsystems (vector modulator, pre-amplifier, klystron):

$$(\sigma_\phi)_{vecMod} = (\sigma_\phi)_{preAmp} = (\sigma_\phi)_{kly}$$
$$= \sqrt{((\sigma_\phi)^2_{total} - (\sigma_\phi)^2_{ref.})/3}$$

For the C-band system the phase tolerance of the vector modulator results in a phase tolerance of the vector modulator of 0.017 deg (rms).

LLRF SYSTEM

The modular 24-channel LLRF system can be split in three groups of components: analog front-end, data converter and digital back-end. The advantage of this modular approach is the well-defined upgrade possibility of individual sub-systems. It also provides flexibility for troubleshooting.

Analog Front-End

The analog front-end consists of a vector modulator, a local oscillator (LO), clock generation, and a multi-channel down-converter. Their design is mainly driven by the required space for the components. The circuit for LO and clock generation and the vector modulator are placed in one 19" chassis with a height of one rack unit while the multi-channel down-converters are placed in a separate 19" chassis. An optical reference system with an optical-to-electrical converter node placed in the LLRF rack will provide a 5712 MHz reference input signal with an integrated jitter of less than 10 fs (10 Hz – 10 MHz).

In the LO unit, the reference signal is divided by 144 to result in the desired intermediate frequency (IF) of 39.667 MHz, which is then mixed with the 5712 MHz reference signal. The extraction and amplification of the upper mixing product provides the required LO signal of 5751.667 MHz at +10 dBm. Along the frequency divider chain the ADC and DAC clock signals of 238 MHz (24th sub-harmonic) are extracted.
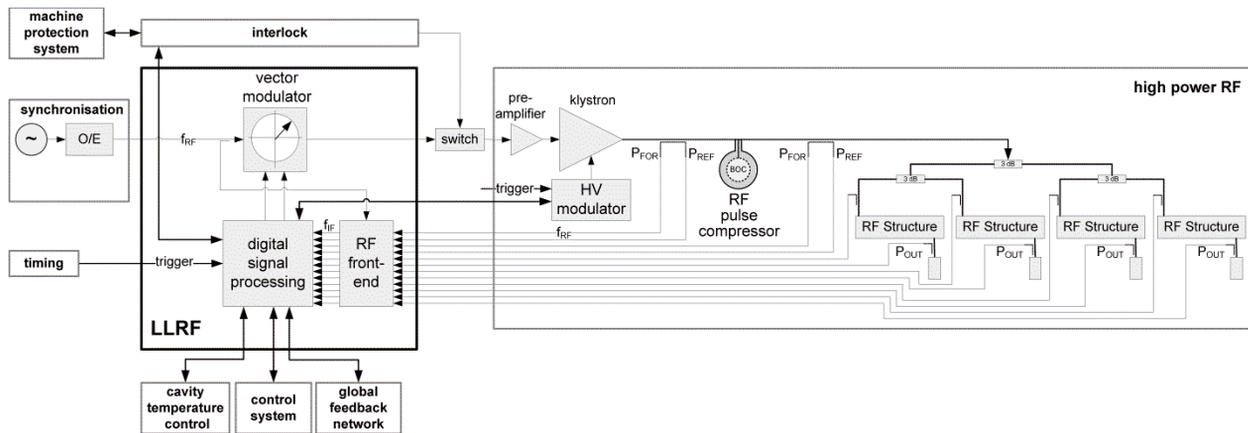
Figure 1: Topology of a SwissFEL C-band RF station
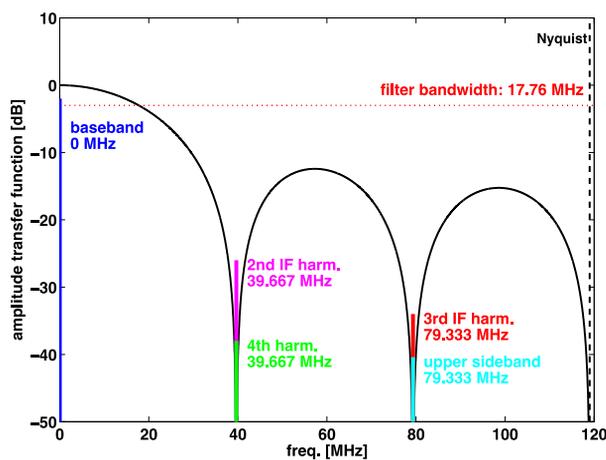
Figure 2: Filter characteristic of non-IQ filter

In a first step, a 16-channel down-converter prototype unit has been developed which down-converts and amplifies the C-band signals (5712 MHz) to an IF of 39.667 MHz at levels of +12 dBm. The unit consists of 4 individual 4-channel receiver modules with additional LO amplifiers on each module. The added jitter of a down-converter stage is around 1 fs (Figure 4).

The vector modulator is designed as a baseband modulator to directly modulate the very clean 5712 MHz reference signal. Therefore the in-phase and quadrature input signals have to be DC-coupled. The common mode spurs from the DACs are suppressed by differential operation amplifiers by 40 dB. The added jitter of the vector modulator driven by the DACs is around 1 fs.

Data Converters

The used data converter boards FMC ADC3110 are commercially available, based on the FPGA mezzanine card (FMC) standard and mounted on a digital FPGA/CPU carrier card IFC1210 [2]. Consequently, they are powered by a switched power supply that supplies the whole VME crate.

Each FMC card provides 8 AC-coupled 16-bit ADCs that are externally clocked with 238 MHz. An ENOB of 11.92 bits and a signal-to-noise ratio (SNR) of 73.5 dB have been reached in the lab. All spurs are 89.95 dB below the carrier at full scale. The channels have at worst a channel-to-channel isolation of 84.2 dB.

The digital-to-analog converter card is a FMC DAC3113 from the same company. The two DC-coupled 16-bit DACs on the board are connected by differential cables to I and Q inputs of the vector modulator in the analog front-end. The performance strongly depends on the spurs generated by the power supply and its filter design on the VME crate's backplane. The SFDR within the 3-dB bandwidth of the DAC (DC to 21 MHz) is at 77.3 dBc and the SNR at 70 dB.

Digital Back-End

The digital back-end processes the raw data of all ADCs, calculates the statistics and provides the data through an EPICS IOC [2]. Signal processing, data archiving and feedback loops are designed to work with 100 Hz repetition rate. For the C-band LLRF prototype system two IFC1210 carrier boards are used with two analog-to-digital converter boards [2].

In the signal processing block the non-IQ algorithm demodulates the digitized IF signals to baseband (I/Q values). The advantage of this type of algorithm is its simplicity with respect to digital implementation issues, and the fact that the generated upper sideband in the digital down-conversion process at $2 \cdot f_{IF}$ as well as harmonics of 39.667 MHz up to a certain degree are automatically suppressed due to the non-IQ filter characteristics (Figure 2) [3]. The selected non-IQ algorithm with an IF to ADC sampling clock ratio of 1/6 provides good synchronization possibilities and results in a detection bandwidth of the LLRF system of about 34 MHz (FWHM). This corresponds to the C-band klystron bandwidth and therefore to the desired monitor bandwidth for fast transient signals like phase jumps after the RF pulse compressor (Barrel Open Cavity, BOC).

The intra-pulse resolution is determined for a user defined time window for every RF pulse. Likewise, pulse-to-pulse statistics are calculated based on a user-defined number of sequent pulses.

SYSTEM CHARACTERIZATION

Amplitude and Phase resolution of the LLRF system is limited by the noise floor at the output of the down-converter, the noise floor of the ADC and the phase jitter of ADC clock and LO signal.

The noise floor of the down-converter measured at the IF port is -137 dBm/Hz. This is 6 dB above the ADC noise floor. For a sampled sine wave the clock jitter introduced by the onboard clock distributor increases the noise floor of the ADC by 2 dB. In contrast, the jitter of the external ADC clock from the LO unit is low enough to have no significant contribution.

The pulse-to-pulse resolution of the whole system is 0.01 deg in phase and 1.5e-4 rel. in amplitude. It is calculated over 100 pulses with an averaging window of 300 ns per pulse. This averaging limits the bandwidth from 0.5 Hz to 1.5 MHz, which corresponds to the filling time of the C-band structures.

The noise floor of the down-converter can be improved by increasing the input signal on cost of the intermodulation distortion of the system. Figure 3 shows the relation between distortion and noise floor as function of the required IF gain. With a chosen IF gain of 27 dB the OIP3 measurement of the prototype down-converter results in a distortion of 0.75 %.
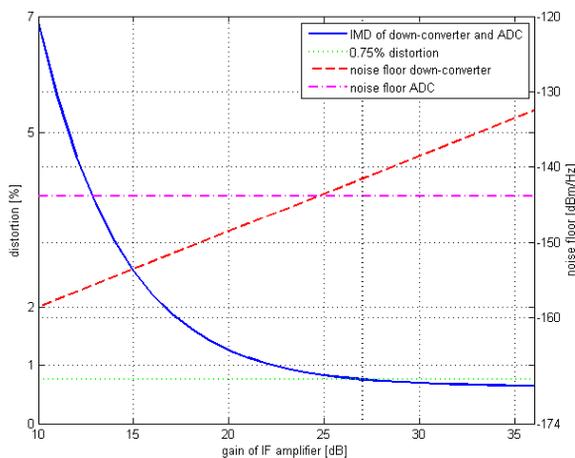
Figure 3: Signal distortion and noise floor of the down-converter as a function of the IF amplifier gain. The noise floor of the ADC is shown in addition.

Channel-to-channel isolation in the down-converter module depends on the RF-to-LO isolation of the mixers and the design of the LO distribution. Since always two channels are driven by one common LO amplifier the crosstalk does not depend on the reverse isolation of the amplifier. After minimizing the leakage of connectorized filters a channel-to-channel isolation of at least 80 dB has been achieved which corresponds to the measured amplitude stability.

Drifts are only important on the receiver side because slow changes on the transmitting path are corrected by the pulse-to-pulse feedback. The analog front-end has a temperature drift of 4.4e-3 rel./°C in amplitude and 2.5

deg/°C in phase. To minimize this temperature dependency the LLRF system is installed in a temperature
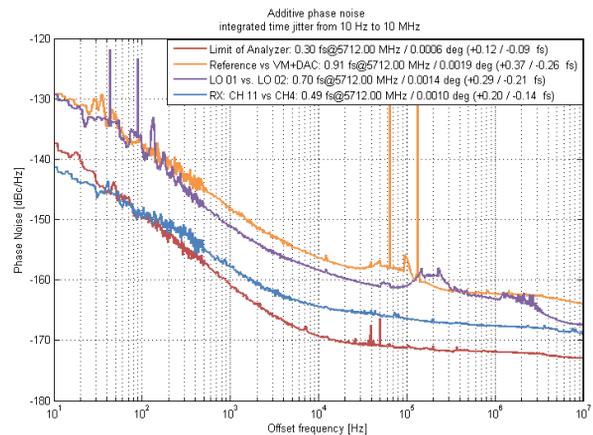
Figure 4: Additive phase noise spectra of VM incl. DAC, LO generation and down-converter

controlled rack at 24 °C ±0.05°C, which is at the same temperature as the accelerator bunker. The expected temperature generated phase drift is therefore below 0.25 deg per day which can be improved by reference tracking. The remaining channel-to-channel phase drift is in the range of 0.1 deg per day. For comparison the present performance of the optical reference signal distribution system limits the phase drift of the reference signal to 0.04 deg per day [4].

CONCLUSION AND OUTLOOK

The prototype LLRF system performs well and is an important step towards the SwissFEL LLRF system. Further attempts are being made to reduce the noise floor of the down-converter to the noise floor level of the ADC on cost on a slightly relaxed distortion requirement of 1%. With this approach and additional filtering of power supplies the measurement resolution of the LLRF will be well below the required RF stability tolerances. The implementation of reference tracking and additional drift calibration will help to improve the channel-to-channel phase and amplitude drift. For the common digital back-end emphasis was put on setting up the firm- and software environment and its integration into the control system. Now, the focus moves on the development of specific LLRF applications.

REFERENCES

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