NEXT GENERATION FAST RF INTERLOCK MODULE AND VME-ATCA ADAPTER FOR ILC HIGH AVAILABILITY RF TEST STATION DEMONSTRATION*

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Abstract

High availability interlocks and controls are required for the ILC (International Linear Collider) L-Band high power RF stations. A new F3 (Fast Fault Finder) VME module has been developed to process both fast and slow interlocks using FPGA logic to detect the interlock trip excursions. This combination eliminates the need for separate PLC (Programmable Logic Controller) control of slow interlocks. Modules are chained together to accommodate as many inputs as needed. In the next phase of development the F3's will be ported to the new industry standard ATCA (Advanced Telecom Computing Architecture) crate (shelf) via a specially designed VME adapter module with IPMI (Intelligent Platform Management Interface). The goal is to demonstrate auto-failover and hot-swap for future partially redundant systems.

INTRODUCTION

The SLAC ILC High Availability R&D program includes controls and instrumentation RF systems, pulsed modulators and DC magnet power. New accelerators and detectors need to take advantage of next-generation enabling technologies to achieve very high availability. ILC studies show that reliability improvement of up to 50 times the components in current use is needed to achieve a (modest) 0.85 overall system up-time [1]. Fortunately, such improvement is possible through new cost-effective (N+1) redundant systems now being applied to physics systems.

The controls and instrumentation electronics platform used for ILC technical and cost modelling is the ATCA Telecom industry open standard, designed for availability at the crate (shelf) level of 0.99999.

SLAC ILC HIGH AVAILABILITY R&D

The ILC R&D electronics program at SLAC includes development of several key technologies aimed at improving reliability and availability and reducing cost of electronics and power electronics systems. Examples are (n+1) redundant modulator and magnet power supply systems [3, 4].

This paper discusses interlocks and controls for high power RF systems. A new Fast Fault Finder (F3) VME module processes both fast and slow interlocks using FPGA logic to detect the interlock trip excursions. This combination eliminates the need for separate PLC control of slow interlocks. F3 modules are chained together to accommodate as many inputs as needed.

In a second iteration of the system the industry open standard high availability ATCA crate (shelf) will be used with a new ATCA -VME adapter module. F3's will be mounted in an ATCA platform featuring IPMI to demonstrate auto-failover and hot-swap to demonstrate a prototype high availability RF station control system suitable for an ILC-scale machine.

A second major goal is a set of ATCA specification extensions to facilitate COTS (Commercial-Off-The-Shelf) solutions to a wide range of new physics machines as well older legacy machine upgrades. This development is being pursued through a new lab collaboration with the industry standards group known as PICMG (PCI Industrial Computer Manufacturer/s Group) [2].

RF INTERLOCK SYSTEM DESIGN

RF System Block Diagram Phases I & II

Fig. 1 shows a simplified block diagram of the RF system interlocks for Phase I. The main components are the klystron, Marx modulator, modulator charging supply, waveguide system to the RF test load and the VME based controls and interlock system. The klystron is a 10 MW peak power L-Band tube operating at a pulse width of 1.5 msec and a pulse rate of 5 Hz. The modulator provides the drive power of 140 A at 120 kV. The modulator together with its charging supply is self-protective.

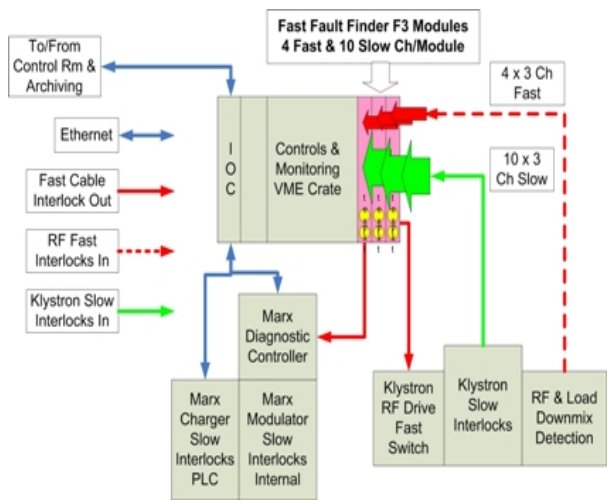

Figure 1: RF Controls and Interlocks Simplified Block Diagram – Phase I.

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The main function of the external interlocks is to protect the expensive klystron from any fault that could cause tube damage, such as an arc fault within the tube or associated waveguide, a failure of the focussing solenoid supply, a heater supply overvoltage or over-current, or cooling system failure. A fast arc fault is the most serious because the modulator HV pulse stored energy discharge could damage or even destroy the tube cathode or grid structure. This energy must be interrupted and diverted away from the klystron within 1-2 µsec of the fault occurrence.

Fig. 2 shows the simplified bock diagram for Phase II in which the F3 modules in the VME crate will be plugged into the ATCA crate (shelf) via ATCA-VME adapters. The adapters are under development with the SAIC Corporation and scheduled for demonstration in early 2010.

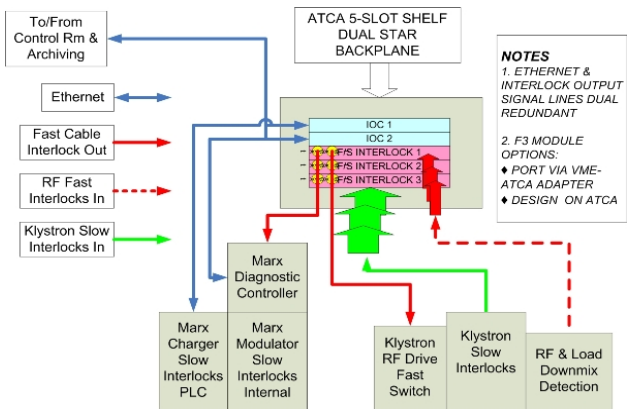

Figure 2: Simplified Block Diagram – Phase II.

Marx Modulator Controls

The Marx modulator has an internal control, monitoring and protection system consisting of a timing and control board on each of 16 cells (HV modules) with fibre optic control and trigger links to each cell from a ground station integral with the modulator [4]. The ground station contains a processor and memory to receive data as well as a link via external Ethernet to the EPICS control system. Each Marx cell has internal protection against over-current and failed switches and a shorting relay that is activated if a cell fails. The Marx control boards have the capacity to sense current and voltage levels within each cell as well as to capture waveforms for diagnostics purposes. The Marx runs stand-alone from a local panel or remotely from the control room.

RF Interlock F3 Module

The F3 VME module processes both slow (DC-50 kHz) and fast (~ 1 µSec response time) interlocks using FPGA high-low threshold logic to detect interlock trip excursions. Each module contains 4 fast and 10 slow inputs, 2 fast outputs for klystron RF and modulator HV abort, and 2 slow DAC outputs for general use. F3 module aborts can be chained together via front panel SMA coax jumper cables to accommodate as many interlock inputs as needed. The F3 is configured and operated from panels in the control room where all relevant date are monitored and archived. The control system also configures and saves FPGA and system parameter configurations. All interlock outputs go to a safe (off=low) condition in case of controls power failure.

F3 Module Details

Fig. 3 shows the F3 hardware. Designed and built at SLAC, the module consists of a single width VME board and front panel and a companion RTM (Rear Transition Module) to bring in the ten slow interlock signals via a SCSI type shielded pair connector. This VME64x module uses a Xilinx XC4VXS35 FPGA as the core logic IC. It also accepts four fast signals via front panel SMA connectors. The four fast signals are sampled at 10 MS/s and the ten DC-coupled slow signals at 2 KS/s rate. All ADC channels are identical units of 8-channel 12 bit serial output ADC's, operated with different clock speeds (decimated clock) and stored to local FPGA memory.

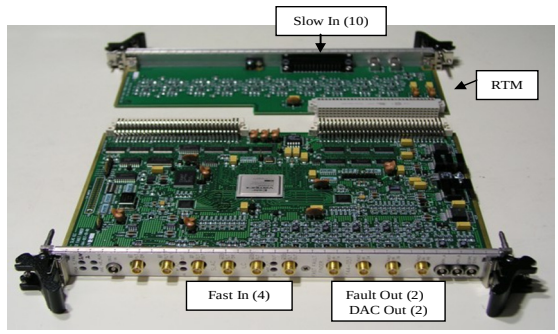

Figure 3: F3 Module Topology.

The module is programmed to compare any fast or slow signals to a pair of threshold levels (low level and high level), one pair per channel, and generate a fault level should a signal deviate outside these preset limits. This fault level is then used to abort operation of either the Marx modulator or the RF drive or both simultaneously.

In addition to the channel low and high limit parameters, a response time algorithm requires that the fault condition be present for a specified time before asserting a fault. A history buffer stores all signal samples which are written to disk when a fault occurs to provide a snapshot of the pre-fault conditions.

EPICS Device Driver

The device driver was written using EPICS operating system independent (OSI) routines. It is presently used with VxWorks and should also work with RTEMS. The device driver is implemented with a set of application programming interface (API) routines to communicate with the hardware. The device support layer allows an input/output controller (IOC) application program to communicate with the driver via a number of EPICS record types. The driver enables read and write access to

module registers and the history buffer memory and handles interrupts generated by the module.

IOC and GUI

The VME interlock system includes three F3 modules, a processor, and 1 each 32 channel ADC and DAC modules. An EPICS IOC is built with VxWorks, device driver libraries for each module, a sequencer program and EPICS autosave utility. The IOC contains a large number of EPICS records which form the database and define process variables (PV's) accessible from Channel Access clients. The system is initialized with the autosave utility which restores setup parameters from previously saved files. Normal operation consists of processing interrupts and operator inputs via the graphical user interface (GUI) implemented as a series of EDM (Extensible Display Manager) screens. Some display fault components; others set up threshold limits, response time parameters, enable selected channels for fault generation, and view history buffer data displayed as waveforms. A select set of PV's are archived with the Channel Archiver channel access client. Figs. 4&5 show two of the many screens.

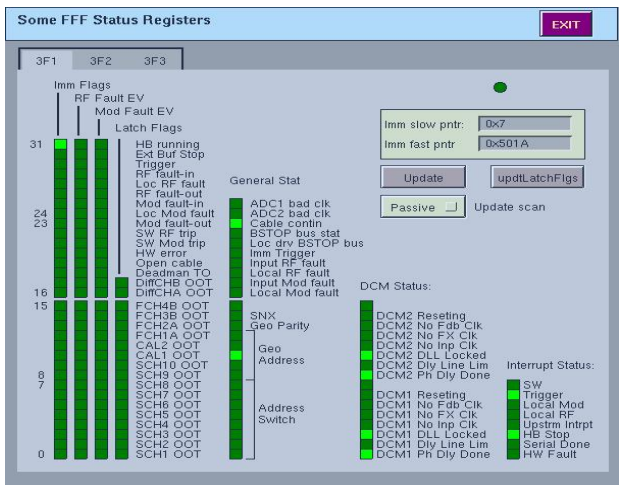

Figure 4: Status Registers.

Figure 5: History Buffers.

Phase II ATCA Adapter Module

The Adapter Module is shown in Fig. 6. The reference design implements IPMI and hot swap features that can be re-used in new designs. All P2 signals on the VME board are brought out to Zone 3 of the ATCA carrier. A new ATCA RTM will be designed for slow signal cable entry.

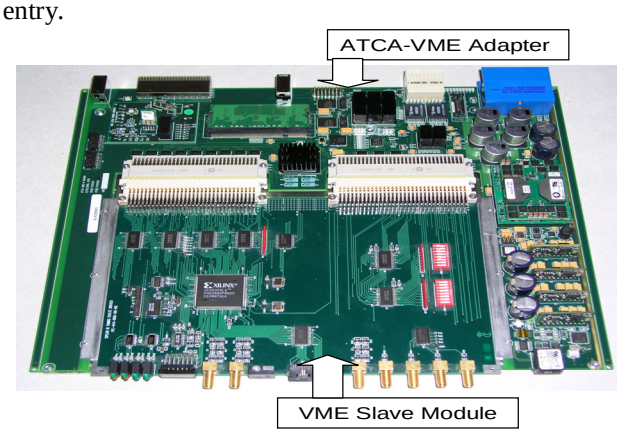

Figure 6: ATCA-VME Adapter Module.

STATUS SUMMARY

The L-Band RF protection system is in process of final checks before connecting to the klystron. The F3 boards are working successfully. Two levels of global protection are achieved by the internal Marx cell protection plus the overall F3 system. The F3's are not redundant but are designed to be failure intolerant and shut down the system safely if control power is lost. The ATCA-VME adapter hardware is complete and the IPMI system is in initial checkout as the first step towards testing with the F3 board.

ACKNOWLEDGMENT

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