THE MACHINE PROTECTION SYSTEM FOR THE LINAC COHERENT LIGHT SOURCE*

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Abstract

A state-of-the-art Machine Protection System (MPS) for the SLAC National Accelerator Laboratory (SLAC) Linac Coherent Light Source (LCLS) has been designed and built to shut off the beam within one pulse during 120 Hz operation to protect the machine from damage due to beam losses. Inputs from beam loss monitors, beam position monitors, toroids, and insertable beam line devices' position switches are connected to a number of Link Node chassis placed along the beam line. Link Nodes are connected in a star topology over a dedicated gigabit Ethernet (GbE) fiber network with a central Link Processor. The Link Processor, a Motorola MVME 6100, processes fault data at 360 Hz. After processing, it sends rate limit commands to two mitigation devices at the injector and another just upstream of the entrance of the sensitive undulator beam line. The beam's repetition rate is lowered according to the fault severity. The SLAC designed Link Nodes support up to ninety-six digital inputs and eight digital outputs each. Analog signals are handled via standard IndustryPack cards placed on the Link Node motherboards with optional interface boards for signal conditioning. A database driven algorithm running on the Link Processor provides runtime loadable and swappable machine protection logic.

INTRODUCTION

The LCLS has been successfully commissioned this year [1] and is producing hard X-rays from the 130 m long permanent magnet undulator at the end of the linac. The sensitive permanent magnet material and other accelerator components are protected from damage by beam losses by a system that shuts off the beam within one beam pulse during normal 120 Hz operation. Fault conditions are monitored by a variety of devices measuring beam loss, beam position, and beam charge together with digital status inputs from beamline insertion devices. The beam is either shutoff or its repetition rate is lowered by either a Pockels cell and shutter at the laser of the photoinjector gun or by a fast abort kicker magnet located just upstream of the entrance to the undulator system. This configuration allows the linac to operate at a steady 120 Hz while the beam rate can be lowered in the more sensitive undulator beamline region whenever faults downstream of the linac are detected.

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ARCHITECTURE

The LCLS MPS uses both commercial off-the-shelf (COTS) and SLAC-built hardware. The system comprises thirty-two Link Nodes covering the 2.5 km machine from the injector laser to the X-ray experimental hutches. At least one Link Node is located every hundred feet for the first kilometer of the LCLS linac; nine Link Nodes are placed around the LCLS undulator. The Link Nodes are connected to a central Link Processor over a dedicated fiber GbE network as shown in Figure 1. The Link Processor evaluates fault conditions and turns the electron beam off at either the gun or the abort kicker just upstream of the undulator according to the state of the machine. The Link Processor and Link Nodes are also connected to the EPICS control network for module setup, monitoring and configuration.

Link Nodes

Link Nodes are the workhorses of the LCLS MPS. They are responsible for debouncing and latching digital inputs, digitizing analog signals and comparing them with fault thresholds, and controlling the MPS mitigation devices. Link Nodes are rack-mountable devices and consume three rack units in a 19-inch rack.

Built around the Xilinx Vertex 4 field-programmable gate array (FPGA), each Link Node can be configured to support up to ninety-six digital inputs, eight solid-state relay outputs, four TTL-compatible logic level trigger inputs, and four trigger outputs. One of each Link Node's two small form-factor pluggable (SFP) slots is filled with a fiber-optic transceiver for high-speed communication with the Link Processor over GbE. A full speed Universal Serial Bus (USB) 1.1 port provides serial communication with the FPGA while a separate DE-9 serial port gives access to the Link Node's EPICS [2] input/output controller (IOC) serial port. The IOC serial ports are connected to terminal servers.

Using a system similar to the bunch purity monitors at Argonne National Laboratory's Advanced Photon Source (APS) [3], Link Nodes use the Arcturus uC5282 embedded microprocessor module [4] as their EPICS IOC platform. The small form factor processor is fitted on the Link Node mother board using a standard 144-pin SO-DIMM connector. The IOC's 100BASE-TX port is used for slower communication with the LCLS EPICS control system.

Link Nodes are configured differently in different sections of the machine. Each Link Node can be config-

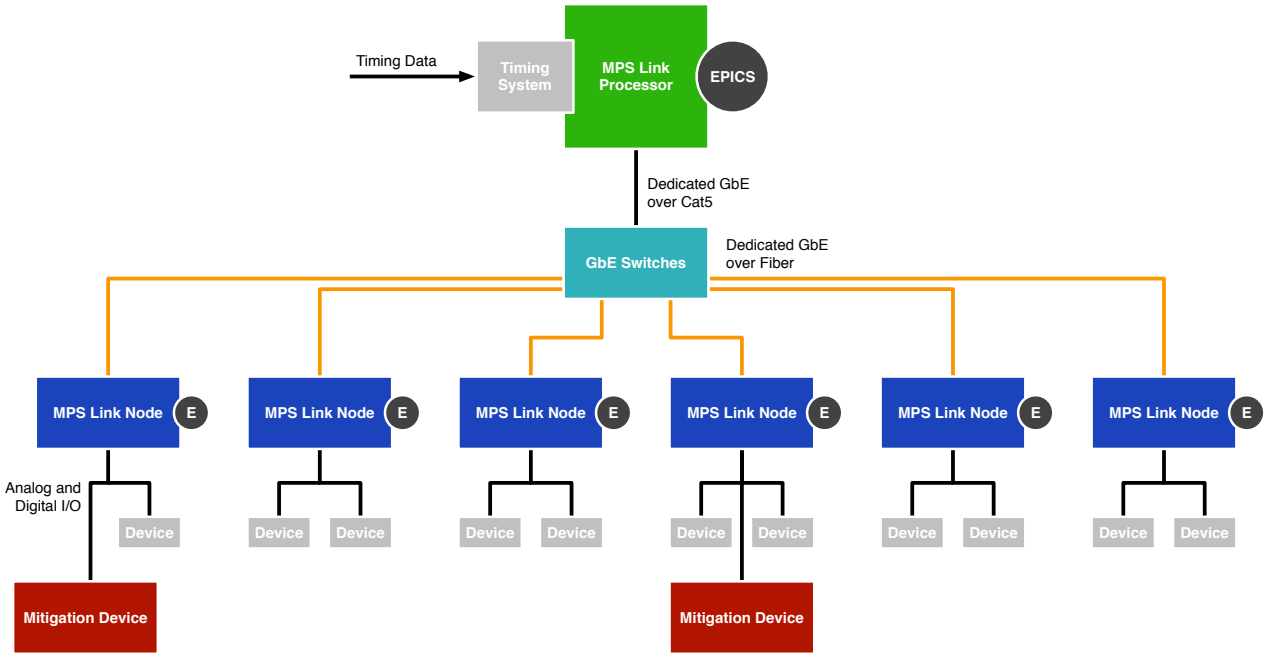

Figure 1: Network overview of the LCLS MPS.

ured with up to six sixteen-input digital input cards and an optional output/trigger card. These cards connect to breakout terminal blocks using DC-37 and DB-25 connectors respectively. Inputs are optically isolated and support SLAC's legacy MPS logic levels of 0/24 V for "fault" and "OK" status.

Four interface board slots allow signal conditioning to be placed between incoming signals and the Link Nodes' IndustryPack cards. COTS analog to digital convertor (ADC) and digital to analog convertor (DAC) IndustryPack Cards are used to control and readback beam loss monitor (BLM) high voltage power supply (HVPS) voltages. A SLAC-designed charge-integrating ADC (QADC) IndustryPack card is used to digitize up to eight protection ion chamber (PIC) or BLM signals, allowing each Link Node to monitor up to thirty-two analog signals. The digitized signals are compared in the Link Node FPGA to thresholds set by the Link Node's IOC via EPICS. Only the boolean results of these comparisons are sent to the Link Processor for fault mitigation.

Link Processor

Link Node fault data is collected by the Link Processor, a Motorola MVME 6100, located halfway down the machine. This VME single board computer has two copper GbE interfaces, a serial console port, and two PCI mezzanine card (PMC) sites. It has a MPC7457 PowerPC processor that runs at 1.267 GHz and has 1 GB of RAM.

Like the Link Nodes, the Link Processor's serial port is connected to a terminal server, one GbE interface is used for high-speed communication with Link Nodes, and the other is used for communication with the LCLS control system.

The Link Processor receives timing information from the LCLS timing system using the Micro-Research Finland Oy PMC-EVR-200 PMC card. The timing software is configured to invoke the Link Processor's communication and fault mitigation code at 360 Hz upon receipt of specific timing data.

MITIGATION DEVICES

The LCLS MPS mitigates fault conditions in less than 8.33 ms using three main devices: a Pockels cell and mechanical shutter to block light from the injector laser, and a pulsed kicker magnet located near the end of the linac to divert the electron beam. The Pockels cell and kicker magnet are able to rate-limit the beam the from 0 Hz to 120 Hz, while the mechanical shutter either passes or blocks laser light.

Each mitigation device is controlled independently allowing multiple beam rates in the machine. The linac can run at 120 Hz, keeping hardware stable, while the rate of electron bunches at the undulator can be limited to 10 Hz.

FAULT COMMUNICATION

All time-critical data is sent over the MPS's dedicated GbE network using UDP/IP. The Link Processor uses a real-time protocol stack (RTS) originally created for the LCLS beam position monitor data acquisition system [5]. The RTS not only provides deterministic behavior for the messaging, but also allows ordinary network hardware and software tools to be used to build and test the system since no new protocols are introduced. On the Link Node side,

the network stack is implemented in the FPGA firmware.

A stack of dedicated GbE switches connects the Link Nodes and Link Processor (see Figure 1). These switches queue and serialize concurrent data sent to the Link Processor and also handle the physical layer conversion of the Link Processor's copper and the Link Nodes' fiber GbE connections.

When the Link Processor is woken by the 360 Hz signal from the LCLS timing system, it broadcasts a synchronization message to all Link Nodes requesting updated fault data, and providing the timing system's newest timestamp. In response, the Link Nodes send the Link Processor a time-stamped status message containing all unacknowledged MPS device faults that have occurred since the last synchronization message. The Link Processor copies the fault data to local buffers and returns the status message to the source Link Node. The Link Node uses this message as an acknowledgement of the faults which the Link Processor has received. All faults are latched in the Link Nodes and are cleared only when the Link Processor has acknowledged the fault and the fault itself has cleared.

The Link Processor processes the faults using the currently running MPS logic and broadcasts a permit message to the Link Nodes. Link Nodes allow beam past their connected mitigation devices for 1/360 s if permitted. If a permit message is not received or if beam is not permitted, Link Nodes stop the beam at their mitigation devices.

While the address resolution protocol (ARP) is supported by both the Link Processor and Link Nodes, it is not required for normal operation. The Link Nodes learn the Link Processor's media access control (MAC) address from the first synchronization message, while the Link Processor learns the Link Node MAC addresses from each received status message. This message ordering also efficiently fills the switches' MAC address tables.

CONFIGURATION CONTROL

Hundreds of fault signals are sent to the MPS and the control room operators need to view the current states and in some cases, bypass one or more of the inputs. Fault status and bypassing is integrated with the rest of the LCLS control system using EPICS process variables (PVs). The large number of input signals are managed with a Relational Database (RDB) which maps each PV to its input channel, card and Link Node chassis. For this task, the LCLS MPS uses the SQLite RDB library.

The SQLite library is unique in that it does not use the common client/server paradigm of other RDBs, but is instead an embedded database engine that provides an SQL application programming interface (API) to SQLite's cross-platform file format. The library has many advantages over the client/server model: there are no servers to setup or maintain, and in many cases no software need be installed before it is used [6]. Because SQLite databases are contained within a single file, they lend themselves to being placed under version control alongside the project's other source code and can be easily shared online.

There are SQLite interfaces for many popular languages, and some languages, such as Python and PHP, package SQLite as a component with their interpreters/compilers.

Python is used extensively in the LCLS MPS project to create files in various formats using the data stored in the SQLite MPS configuration files. The LCLS MPS Python module exports EPICS database (.db) files, .edl files for use with the EDM graphical user interface, state notation language (SNL) code, C header files for use with MPS logic, LaTeX documentation, and finally, comma separated value (CSV) files for use in non-SQLite applications.

MPS LOGIC

MPS logic is built by specifying truth tables that provide the maximum allowable beam rates at mitigation devices given the status of their inputs. Where truth tables are not practical (for example: a truth table with more than sixteen states), C code can be embedded to determine maximum rates. Logical expressions are evaluated on the Link Processor at 360 Hz, just before the permit message is broadcast to the Link Nodes.

Each version of the MPS logic is stored in a separate SQLite database, and, like the configuration database, a Python module exports the data to various files. The most important of these files is the C code which is compiled into runtime-loadable object files for the Link Processor. These object files contain the set of truth tables for the Link Processor to evaluate.

Up to sixteen logic objects can be loaded on the Link Processor at once. Three PVs are used to manage the logic objects: one to load, another unload, and the last to select which set of truth tables should be evaluated.

As with the configuration database, a Python module exports LaTeX documentation describing the truth tables in an easy-to-read, searchable format.

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