FIRST FULL-SECTOR CLOSED-LOOP OPERATIONAL EXPERIENCE FOR THE FPGA-BASED BROADBAND BEAM POSITION MONITOR AT THE APS*

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Abstract

The Advanced Photon Source (APS), a third-generation synchrotron light source, has been in operation for eleven years. The monopulse radio frequency (rf) beam position monitor (BPM) is one of three BPM types now employed in the storage ring at the APS. It is a broadband (10 MHz) system designed to measure single-turn and multi-turn beam positions, but it suffers from an aging data acquisition system. The replacement BPM system retains the existing monopulse receivers and replaces the data acquisition system with high-speed analog-to-digital converters (ADCs) and a field-programmable gate array (FPGA) that performs the signal processing. The new system has been installed and commissioned in a full sector of the APS. This paper presents the results of testing the beam position monitor, which is now fully integrated into the storage ring orbit control and fast feedback systems.

INTRODUCTION

A full sector of rf BPMs at the APS has been upgraded to the new FPGA-based signal processing electronics. As fully described in [1], the upgrade replaced only the data acquisition portion of the system. This was accomplished by physically separating the existing monopulse receiver from the signal conditioning and digitizing unit (SCDU) [2] data acquisition electronics, repackaging the receiver in a custom EMI-shielded chassis, and replacing the SCDU with a custom C-sized VXI data acquisition module. A set of thumbwheel switches on the front-panel specifies the sector number and letter of the unit. The IOC name (of the form iocs38abpm) and network IP address are set using the value read from these switches. This makes it easy to swap out a failed unit.

DIGITAL SIGNAL PROCESSING

The digital signal processing operations carried out by the FPGA firmware are shown in Figure 1. Several firmware changes have been made from the versions previously reported. The most significant differences are that the conversion to engineering units is now done in the FPGA and that the linearization polynomials are now applied in all the computation chains. The former change reduces the load on the EPICS input/output controller (IOC)[3] on the module, and the latter ensures that all position values are computed in the same fashion.

The sum and position signals for each plane are first processed by a group of low-pass filters that result in six streams of data, one for the fast feedback system, two for the noise power calculations, and three that are later used to provide sets of EPICS process variables (PVs) labeled ms, msAve, and mswAve for historical reasons. All six streams are passed through a linearization block that performs pincushion correction by applying the polynomials shown in equations (1) and (2):

$$x' = x + C_{x12}xy^2 + C_{x30}x^3, \quad (1)$$

$$y' = y + C_{y12}yx^2 + C_{y30}y^3. \quad (2)$$

The x and y values are the raw position values from the filter blocks and x' and y' are the linearized position values sent to the EPICS process variables, the fast feedback system, and the rms computation chains. The polynomial coefficients are set on a per-BPM basis to account for the various chamber geometries used in the APS storage ring. Although there is only a single linearization block in the FPGA, it does not present a significant bottleneck since the implementation is fully pipelined and capable of producing a pair of linearized values on every clock cycle. As well, the values for the fast feedback system are given priority, thus minimizing the latency in forwarding these values to the fast serial link transmitter. The IOC contains a table holding the polynomial coefficients for each type of chamber in which IOC buttons are located. The FPGA sends beam position information to the fast feedback system over a dedicated 100-Mb/s fiber link. The FPGA continues to perform this operation even when the embedded IOC is rebooted. This minimizes the effects of IOC software, hardware, or network faults.

The values of the raw, adjusted, and error values for the PVs mentioned above are calculated and made available to the IOC. The ms and msAve PVs have 10-Hz and 1-Hz signal bandwidth, respectively, and are updated at 10-Hz, whereas the mswAve PVs have 0.1-Hz bandwidth and are updated at 1 Hz. The rms variation of the sum and position signals in the frequency ranges 1-Hz to 200-Hz and 1-Hz to 5-kHz bandwidths are calculated and made available as PVs.

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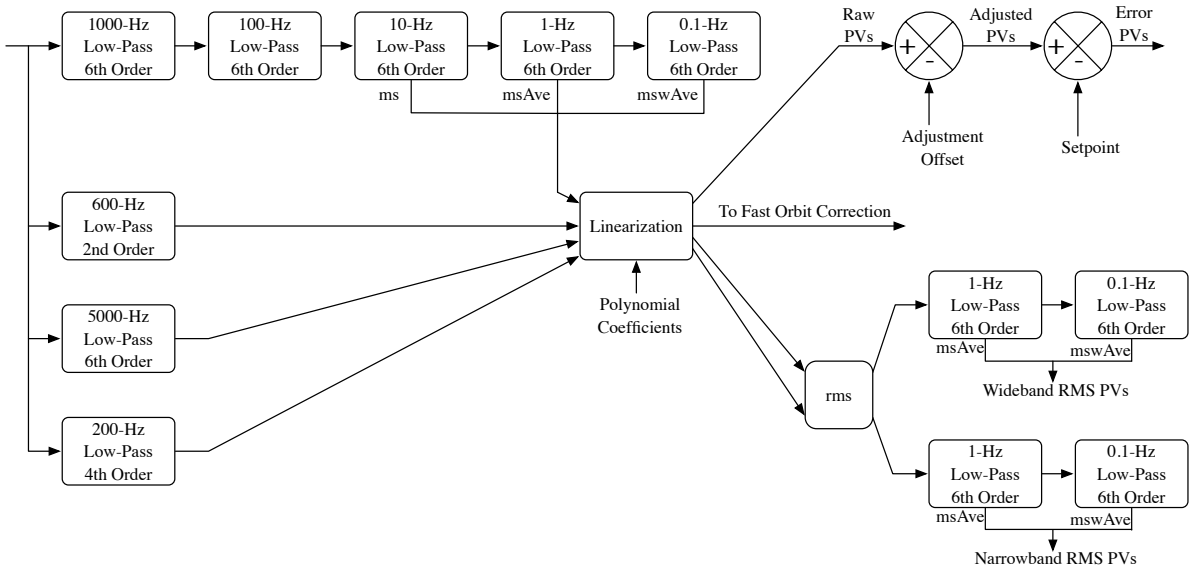

Figure 1: Signal processing firmware.

WAVEFORM RECORDERS

There are four separate waveform recorders in the FPGA:

1. An 'oscilloscope' that records the raw signals from the analog-to-digital converters (ADC) at the full sampling rate of 88 MHz. The waveform buffers are 4096 samples deep with an equal number of pre and post trigger samples. This recorder has been invaluable in tracking down problems with the monopulse receivers.

2. Up to 262144 samples of the turn-by-turn average of the sum and position ADC values taken at the storage ring turn rate of 272 kHz. The trigger position can be selected to be at any location within the buffer.

3. Up to 2048 samples of the raw 'ms' PVs taken at a 100-Hz rate. The trigger position can be selected to be at any location within the buffer.

4. A single-turn sample of the turn-by-turn average of the sum and position ADC values.

The recorders can be triggered by the APS event system, by EPICS or in the case of the turn history recorder, by the value of a sum channel value falling below a specified threshold.

PERFORMANCE

Figure 2 shows the frequency spectrum of the beam horizontal motion during normal (24×1) storage ring operation. The spectrum was computed by applying the fast Fourier transform (FFT) to a waveform record acquired by the turn-by-turn recorder in the FPGA. The large number of points in this waveform record allows a single acquisition to provide information from approximately 1 Hz to the Nyquist frequency of 135 kHz. The limited amount of memory on the embedded IOC and its lack of floating point instructions requires that the FFT be performed off-line. The effects of AC line noise through the twelve phase rectifiers in the klystron high-voltage power supplies can be seen as the 720-Hz component at the left of the graph. The component at approximately 1.8 kHz is the synchrotron oscillation. The large component at 40 kHz is due to the switch-mode magnet power supplies. The fractional horizontal tune can be seen as the lines at approximately 32 kHz.

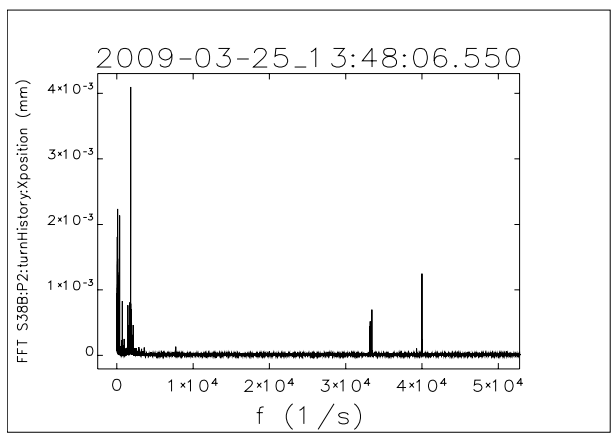

Figure 2: Spectrum of beam horizontal motion from 1 Hz to 50 kHz.

The system noise floor was determined by combining the signals from the four buttons of a BPM into a single signal, then splitting that signal equally into four signals applied to the input of the filter/comparator module. This effectively

removes the effect of beam motion and allows the end-to-end noise floor to be measured. The noise spectrum of a turn history acquisition during normal (24-bucket) machine operation is shown in Figure 3. The noise floor in a 1-Hz to 200-Hz band is less than 160 nm. The conversion to distance units is based on the vertical conversion factor for a standard elliptical storage ring chamber. For an 8-mm chamber the noise floor improves by a factor of 6.5 (noise floor less than 25 nm).

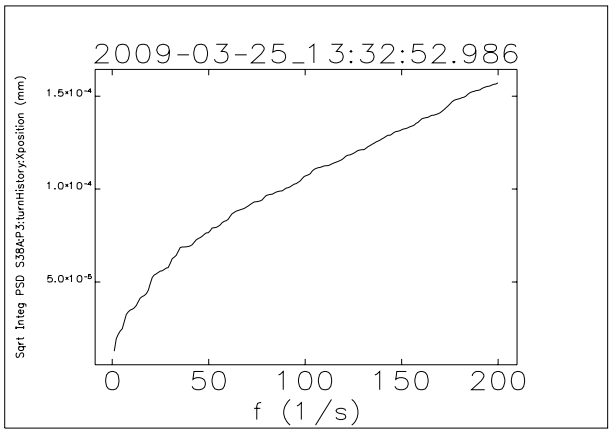

Figure 3: Full system (Buttons to FPGA) noise floor.

An example of the turn-history capture capabilities of the unit is shown in Figure 4. The full turn-history capture extends to almost one half second on either side of the trigger point. Only the portion of the recording beginning about 20 ms before a beam dump is shown in the figure. The turn-history plot shows a fast disturbance which excites an approximately 1.8-kHz oscillation. The cause of this is likely a disturbance in the storage ring rf amplitude or phase.

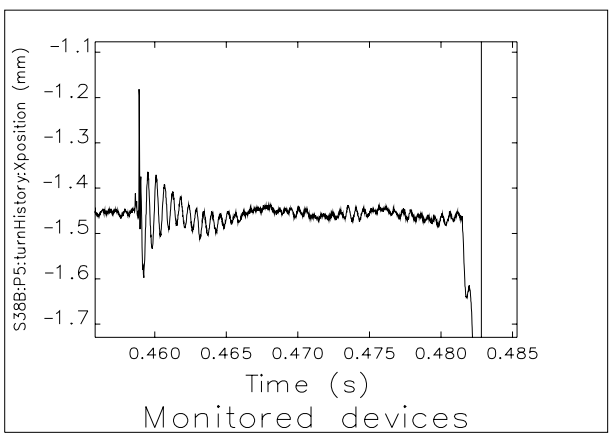

Figure 4: Turn-by-turn record of beam horizontal position preceding a beam dump.

The data acquisition portion of the FPGA firmware provides great flexibility in selection of samples to be used to compute the turn-by-turn averages as well as control of the X/Y plane switching and commutation signals to the monopulse receivers. This flexibility comes at a cost, however, in that it proved to be very tedious to set up the configuration parameters for each storage ring fill pattern. A GUI-based tool has been written that greatly reduces the effort required to set up an acquisition and processing control pattern. The tool can obtain live data from the oscilloscope waveform recorder and display the timing relationship between these samples and acquisition control pattern. This makes it easy for an operator to choose the samples to include in the beam position calculations.

During testing it was found that the number of simultaneous EPICS clients was limited by the amount of memory set aside for the real-time operating system on the IOC. An upcoming release of the operating system on which the IOC application runs will remove this limitation and not restrict additional clients until all memory on the IOC has been exhausted.

The logarithmic amplifiers used in the monopulse receivers are not identically matched. This leads to an apparent shift in beam position for different beam intensities. The problem is most apparent when the ring is operating in 'hybrid' mode with a larger number of electrons in one bunch relative to the other bunches. We are investigating the possibility of adding logic to the FPGA to compensate for these effects.

CONCLUSIONS

A full sector of APS beam position monitors has been upgraded to FPGA-based data acquisition and signal conditioning hardware. The new hardware has been used to successfully close the loop of both the slow and fast orbit control feedback systems. No problems with either the FPGA or the embedded IOC have been noted. Additional sectors will be converted to the new system during upcoming maintenance periods.

REFERENCES

[1] A. Pietryla, H. Bui, G. Decker, R. Laird, R. Lill, and E. Norum, "Status of the RF BPM upgrade at the Advanced Photon Source", *Proceedings of the PAC07*, Albuquerque, New Mexico, 2007, FRPMN116, p.4390 (2007); http://www.JACoW.org.

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[3] *uCdimm™ ColdFire 5280/5282 Hardware/Firmware Reference Guide*, Arcturus Networks Incorporated, 116 Spadina Avenue, Suite 100, Toronto, Ontario, Canada, M5V2K6.