# PROTOTYPE BEAM POSITION AND PHASE MONITORING ELECTRONICS FOR LANSCE\*

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#### Abstract

Future improvements to the Los Alamos Neutron Scattering Center (LANSCE) include new beam position and phase measuring systems that operate at 201.25 MHz. An effort is underway to build and test prototype electronics for these applications. We plan to use direct down conversion to 115 MHz followed by COTS FPGA hardware for in-phase and quadrature-phase (I/Q) signal processing. Self-calibration and system diagnostics circuits will be included. We are reporting on the status of these efforts.

## **INTRODUCTION**

At LANSCE we are planning a significant upgrade to the machine diagnostics in the near future. Included in the scope of this upgrade is the installation of approximately 30 new beam position and phase monitors (BPPMs) in the linac [1,2]. The fundamental requirements for this system are listed in Table 1.

Table 1	: Approximate	BPPM	System	equirements
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Parameter	Requirement		
Frequency	201.25 MHz		
Measurement bandwidth	80 kHz		
Position accuracy	$\pm 2.5$ % of aperture		
Position resolution	0.25 % of aperture		
Phase linearity	±0.25 degrees		
Phase resolution	0.25 degrees RMS		
Beam current range	0.9-21 mA		
Signal power range	-58 to -5 dBm		

Features we want to have in the electronics system include built-in channel gain calibration, channel phase calibration and cable continuity verification.

As of this writing we are considering two sources of BPPM system electronics. These are 1) an in-housedesigned version using custom analog front end and ADC circuits followed by a National Instruments FlexRIO® FPGA processor module and computing system and 2) a commercially-available Libera® system from Instrumentation Technologies with application-specific modifications [3]. This paper reports on our efforts towards the first approach. The Libera® testing will start later this year when additional funding becomes available.

# **BPPM ELECTRONICS TOPOLOGY**

The prototype BPPM electronics system currently being fabricated consists of five main parts. These are the

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Instrumentation

input module, the ADC-to-FlexRIO module, the FlexRIO module, the PXIe crate and computing system and the rf reference generation chassis.

## Input Module

The input module has four inputs for the BPPM signals, and a calibration reference input. It has outputs for the four channels, plus four dc voltages that are proportional to the dc resistance to ground at the input of each channel.

A 4-by-4 cross-point switch is included right before the module outputs, which allows any input to be connected to any output. This can be used in the event that one wishes to use the beam signals to calibrate the four signal channels. This would theoretically be the most accurate method of calibrating the BPPM system.

The calibration input goes through a switchable attenuator and then to a four-way multiplexer to each of the four signal channels. This calibration signal can be connected to either the module input, and thus to the cable going to the BPM on the beam line, or it can be switched into the input of the signal channel while disconnecting the BPM input signal. Like previous BPM systems we designed for SNS, this allows for calibration of the BPM cables and lobes via the time-domain-reflectometery technique [4-6]. This calibration method does not require the beam to be present and can also be used to verify the operation of the system when beam is not available. All circuits on this module are designed to operate in excess of 805 MHz should we wish to process beam signals at other beam harmonics in future applications. Prototypes of the needed sub-circuits have been built and tested. The RF chain, minus the crosspoint switch, is shown in Fig. 1.



Figure 1: The prototype board with sub-circuits for a single channel of the input module. The circuits include all of the RF switching except for the crosspoint switch.

The input circuit is expected to be built into a PXIformat module and installed next to its companion FlexRIO module.

### ADC to FlexRIO Module

The ADC to FlexRIO module will have four channels of Linear Technology, LTC2208, 16-b, ADCs with low-distortion input rf amplifies. The rf outputs from the input module drive these four inputs. The 64 LVDS ADC outputs, plus the data valid clocks, will connect to a card edge connector that mates with the FlexRIO module and hence, directly to the ZilinxVirtex-5 FPGA within.

We developed and tested the prototype ADC circuit card earlier [3]. This circuit needs to be transferred to the new ADC to FlexRIO adapter card. The prototype ADC card is shown in Fig. 2.



Figure 2: The custom four-channel AFE using Linear Technology LTC2208 ADCs. RF inputs are on the left and connections to the digital I/O cards are on the right.

We have just finished collaborating with New Mexico Tech University and National Instruments to develop a matting FlexRIO adapter card. The adapter takes the signals from our ADC card over LVDS cabling and ports them to the FlexRIO module. This adapter is shown in Fig. 3. We will use this for testing the interface and for developing the initial FPGA code for BPM signal processing. Students at New Mexico Tech University have already written and tested the first generation FPGA code.

We have not taken delivery of this adapter card as of this writing. After testing is completed, a new module will be designed which incorporates the amplifiers and ADCs on a single card that plugs onto the FlexRIO module without using any cabling.



Figure 3: The custom FlexRIO adapter module designed to connect the ADC card to the FlexRIO module.

#### FlexRIO Module

The FlexRIO module is a new National Instruments PXI module that contains a Xilinx Virtex-5® FPGA. The I/O pins of the FPGA connect to a card edge input connector on the front of the module, allowing custom hardware to be designed with direct access to the FPGA. The FPGA is programmed via LabVIEW® FPGA software. The module is available with different variants on the Virtex-5 family as needed by the application.

In our BPPM system, we use 64 LVDS channels to transfer the outputs of the four ADCs to the FPGA, plus a few miscellaneous timing signals and binary I/O.

### PXIe Crate and Computing Platform

The FlexRIO® and input modules plug into a PXIe crate also that contain the crate controller, accelerator timing module and perhaps a generic DAQ module if needed.

We expect to eventually run LabVIEW RT on the controller, which will also run the EPICS server.

#### **RF** Reference Generator Chassis

The RF reference generator chassis will take in the 201.25 MHz acceleration system reference which is distributed throughout the linac. From this it will create the ADC sampling clock at 115 MHz, the I/Q reference at 28.75 MHz and a replica of the 201.25 MHz input to drive the calibration input of the BPPM.

A separate RF reference chassis will be required for each location in which we install BPPMs. Currently we do not need to make absolute phase measurements with the BPPM system, so all of the systems will be run asynchronously from each other. If absolute phase measurements are required, the I/Q reference would have to be distributed to all BPPM systems from a common source.

If we choose to measure beam position and phase at 402.5 or 805 MHz, we would also need to create those frequencies from the 201.25 MHz input. We do not plan to do this at this time, however.

#### **DEVELOPEMENT STATUS**

At this time we have built and tested a prototype of the ADC circuits and their required low distortion rf drive amplifiers. The performance of these circuits meets or requirements.

We have built and tested the various sub-circuits that will be incorporated into the input module and the schematic has been submitted to our ECAD team for PCB design. Individually, these sub-circuits meet our requirements.

The New Mexico Tech University team, along with National Instruments, have designed a FlexRIO adapter card that connects our prototype ADC card to the FlexRIO module. They have written the FPGA code necessary for the FlexRIO module to process the ADC outputs and calculate beam position and phase. We at LANL will receive this hardware and software shortly and begin our own testing and development.

We have the National Instruments PXIe-1062Q chassis, PXIe-8106 embedded controller and PXI-7951R FlexRIO module in hand and operational.

No work has been done on the RF reference generator chassis to date. We expect to have a complete BPPM system up and running this summer, minus the RF reference chassis, which will probably follow in the fall when we receive additional funding.

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