DEVELOPMENT OF A FAST SIGNAL-GATING CIRCUIT FOR OBSERVATION OF FAST GLITCH OF PHOTON BEAM INTENSITY AT NSRRC

Fu-Tsai Chung#, Meng-Shu Yeh, Chaoen Wang, Ho-Ping Chang,
Yi-Chih Liu ,Yu-Hang Lin, Yao-Kwang Lin, Chih-Hung Lo
National Synchrotron Radiation Research Center,Hsinchu,30076,Taiwan, R.O.C

Abstract

Stability of photon beam intensity, I_0, is one of the most important performance merits of a modern light source. The photon intensity measured at dragon beam line (BL11) is routinely used as a reference signal for I_0 stability measurements. At NSRRC, a highly stable I_0 intensity is maintained in most percentage of the user beam time. Meanwhile, glitches of I_0 intensity up to few tens of percentage had been observed once every few operating hours, which was a puzzle before its reason had been identified later. A spontaneous large variation of photon intensity $\delta(I/I_0)$ caused difficulties for users operating their experiments. Here, we report our development of a dedicated electronic circuit with functionality of single-gate, which was very helpful to clarify the puzzle of I_0 glitches observed at NSRRC.

INTRODUCTION

Discovering the reasons for I_0 glitch required direct evidence to discover the perturbation sources that caused the I_0 glitches. Whenever we understood those reasons, we diminished the glitches of photon intensity. Meanwhile, how to identify the possible perturbation sources is not trivial. Obviously, an orbit spike will cause a glitch of the photon beam intensity. The orbit glitch may be due to spontaneous malfunction of some non-identified corrector power supply. On the other hand, whenever the global orbit feedback system is spontaneous out of control due to some unknown bug of software, an orbit glitch will be generated. Because the occupancy of the I_0 glitches was not frequently enough to clarify the suspicion of global orbit feedback by switching it off during the available machine study time for a mature operating light source.

Software solution is inadequate to clarify our question because of the slow sampling rate of the data acquisition database available at NSRRC; the other is the design of specific hardware to identify the sources of I_0 glitches, for which objective we must record immediately the complete real-time information from observing the related signals. Our designed hardware circuit not only provided high-speed sampling but also decreased the noise effect. Hereafter, we report our development.

THE STRUCTURE OF HARDWARE

The hardware structure acquires the correct signals, timing and signal source. Figure 1 shows a block diagram of the home-designed hardware architecture that comprises analogue signal processing, a digital filter, an amplifier, a synchronous trigger signal and a timing trigger. The hardware structure provides a new solution to restore the signal after aliasing; this solution is called a gating function.

Such a gating function was designed and divided into several parts with this structure:

- signal source amplification and noise reduction, by differential circuit
- synchronous trigger source
- digital filtering
- hardware synchronous timing
- home-designed mask circuit, and
- Analysis with oscilloscope.

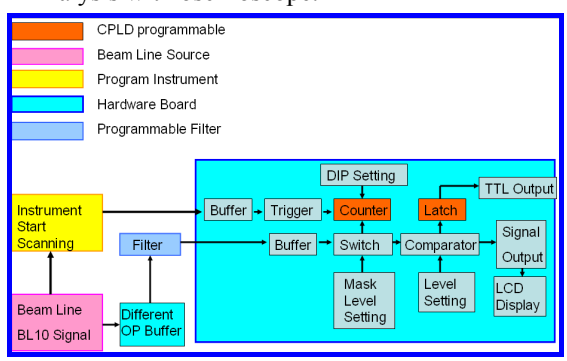

Figure 1: The home-designed hardware architecture.

CIRCUIT BOARD

Differential Circuit

The distance between the source of the I_0 signal (located at BL11) and the location of observation (a SRF rack in the core area) is about 45 m. The I_0 signal is wired to a junction box on the SRF rack and connected to a diagnostic system. The distance 45 m is a challenge for signal propagation, especially for a small signal such as I_0. Along the path between BL11 and the SRF rack, there are many power lines; the 60-Hz oscillation of the power might cause EMI of the I_0 signal. Interference of this kind is solved with an interference reduction circuit as shown in Figure 2. An integrated circuit (IC, AD620), acting as a differential amplifier with unit gain, serves in the circuit to reject interference.

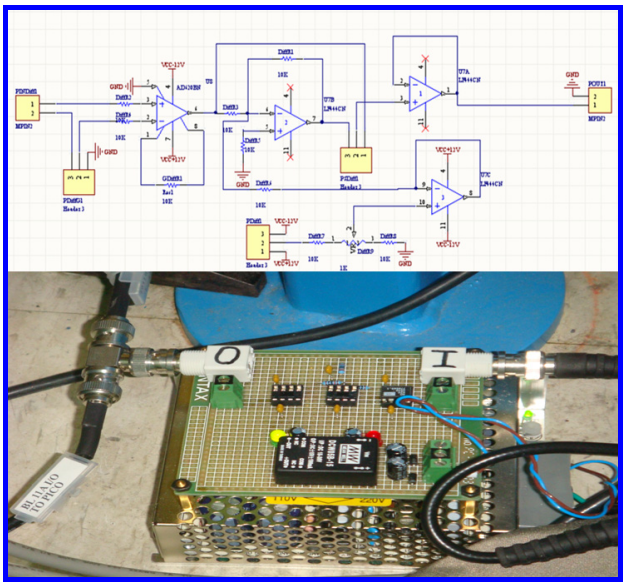

Figure 2: Differential circuit.

Trigger Synchronization

When the I_0 measurement instrument switches to a scanning mode, the diagnostic system must synchronize the timing of the switching. A trigger source is thus required for the diagnostic system, but the original trigger source, from the instrument and control group, has negative pulses with extremely narrow time period (about 400 ms) as shown in Figure 3. The low-level oscilloscopes can not take such signal as a trigger source because of the narrow time period and the 45-m travel. To solve this problem, we designed a transform circuit to transform the signal in the narrow time period to a standard falling-edge TTL signal. The TTL output of this circuit can thus serve to trigger the oscilloscopes.

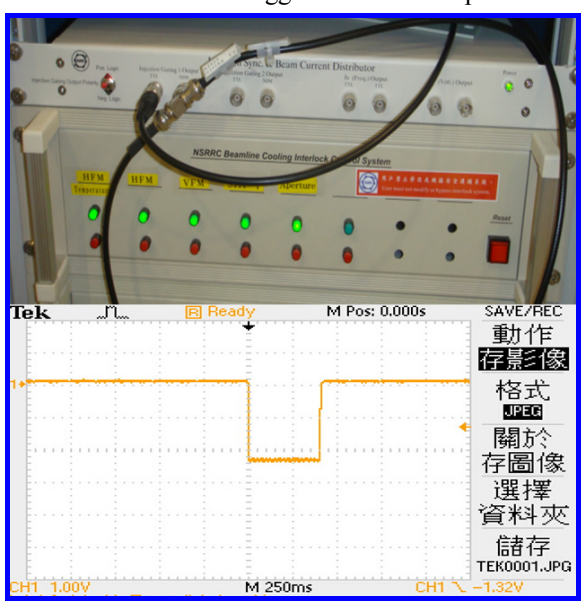

Figure 3: Trigger signal.

Digital Filtering

Many unwanted signals are located in various frequency bands at the output of an interference reduction circuit. To reject these alien signals and to purify the I_0 signal, we use a low-pass digital filter (Frequency Device INC 90IP) to exclude signals with frequency above 30 Hz. Figure 4 illustrates the digital filter.

Figure 4: Frequency Device INC 90IP Filter.

Timing Module

We designed a module for a timing recorder, which records the real clock of a trigger event, as shown in Figure 5. The real clock, specifying year, month, date, hour, minute and second, can be manually set. A memory, which is erasable and reusable, is installed in the timing module. To activate the timing recorder, a falling-edge TTL trigger signal is needed. The gating function provides such a TTL signal to activate this module. When the timing device acquires the error information, it stores a timing message in its memory. This module is convenient for tracking the timing of glitch of photon intensity.

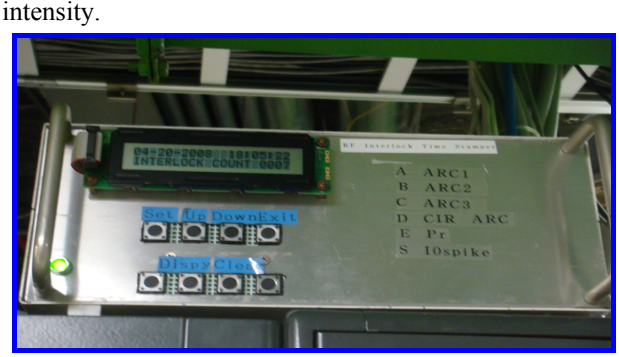

Figure 5: Home-Design Timing Recorder.

Mask Generation Circuit

The scanning mode of the I_0 instrument, in which 10~15 s are needed to complete the mathematical calculations, makes the I_0 signal unstable, which corrupts an analysis. To catch accurately the glitches appearing in

the I_0 signal, a mask generation circuit was developed to block a signal in the scanning mode period of which the I_0 signal is floating and useless for analysis.

The temporal resolution of a digital circuit can be as great as microseconds, which is helpful to design a mask-generation circuit with fine time resolution. A complex programmable logic device ALTERA (EPM7064SLC44-10) is employed as the core of the mask generation circuit. Instead of the I_0 signal, an adjustable reference bias is output within the blocking period. Accordingly, the CPLD is configured as a controller of the output signal switch between the mask reference bias and the I_0 signal. A smoothly adjustable reference bias is generated with an integrated circuit (LM385AXZ-2.5), and a digital switch (DG412) with switching time less than 175 ns is employed.

As shown in Figure 6, the trigger source generated by the trigger synchronization circuit has a period 60 s. As the mask generation circuit receives a TTL signal from the trigger synchronization, the circuit generates a posterior mask for 6 s. After that, the circuit outputs a low state until the fifty-sixth second of every trigger cycle. At that point, i.e. 4 s before the next trigger, a prior mask is generated that covers fully the 10-s scanning period. The signal within the mask period becomes blocked to ensure the accuracy.

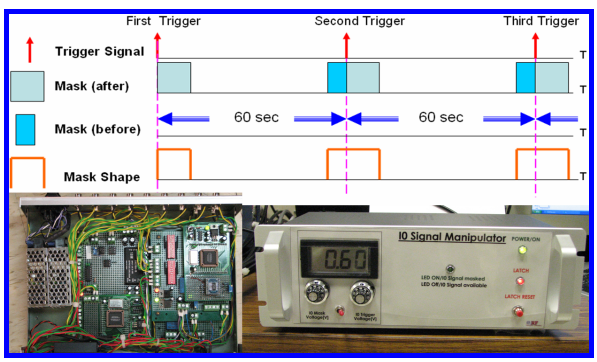

Figure 6: Home-Design Mask Generator Function.

SUMMARY

Occasionally appearing error sources are difficult to track. A gating function has been developed and employed to detect and to identify the possible error sources. With the aid of this gating function circuit, the functionality of global orbit feedback system was removed out from our list of suspicious error sources. Later on, data acquisition software has been implemented with new functionality to identify the global orbit distortion during I_0 glitches. Orbit correction software developed by one of the author (HP Chang) was used to identify the possible location of the error sources. We discovered that I_0 glitches were caused by the SWLS feed-forward system, including the side-coil and two correction coils, triggered by the reading error of the main power supply. The problem was thus solved by our control staff.