LCLS STRIPLINE BPM SYSTEM COMMISSIONING *

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Abstract

The Linac Coherent Light Source (LCLS) began x-ray laser operation this year. Stripline BPM system requirements include position resolution better than 5 microns for single-bunch beam charge of 200 pC. We describe the processing scheme, system specifications, commissioning experience, and performance measurements.

INTRODUCTION

The LCLS requires better BPM resolution at lower beam charge than did previous users of the SLAC linac. We estimated that the existing BPM striplines could be used with a redesigned BPM processor to achieve the required resolution (Table 1) with improved systematics. We chose to implement the processor by developing a four-channel analog front-end (AFE) board to shape, amplify, and provide calibration of the stripline BPM signals for digitization on a 4-channel waveform digitizer board developed for LCLS low-level RF.

Table 1: LCLS BPM System Requirements

Parameter	Value	Comments
Dynamic Range	0.08 – 8 nC	40 dB
Resolution	5 microns	@ 0.2 nC
Stability	5 microns	Over 1 hour

Requirements and Simulation

The BPM processor shapes and digitizes the stripline signals. The signal acquisition is expected to perform over a 0.08 - 8 nC dynamic range with a resolution better than 5 microns at 200 pC and stability of less than 5 microns offset drift over an hour.

Calculations in MathCAD and Matlab, and simulation in SystemView showed that the processor should have a few low-noise RF amplifiers, an overall gain about 34 dB, a relatively broadband front filter and a narrow band backend filter. Programmable attenuators, distributed between amplifiers, are adjusted for optimal gain while keeping amplifiers out of saturation [1].

ANALOG FRONT-END

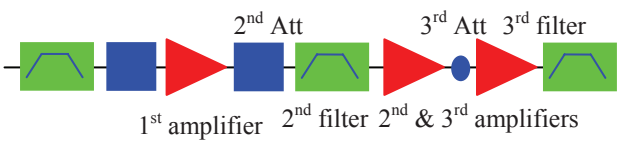

Figure 1. One channel of the analog frontend.

Three RF amplifiers and three band-pass filters provide low noise amplification with gain programmable by two digital attenuators per channel, providing a total dynamic range control of 46 dB (Figure 1).

Two different lengths of stripline pickups are used in LCLS: the typical linac BPM strips are 10 cm long, while the striplines intended to provide higher resolution for the linac-to-undulator section are 50 cm long. Due to the difference in frequency response of the two type of striplines we build BPM processors at two different center frequencies, 140 MHz and 200 MHz. Band-pass filters define a bandwidth of 7 MHz at the operating frequency, either 140 MHz or 200 MHz, of the board.

Online Calibration

The BPM processor continuously self-calibrates between beam pulses (Fig. 2). The AFE transmits short (~260 ns) tone-bursts at the processor frequency alternately on one of the striplines on each of the BPM axes (typically the Y^+ and the X^- striplines). The ratio of amplitudes of the signals detected on the two adjacent striplines calibrates the gain ratio of these processor channels and their associated cables. The calibration drive amplifier can put out as much as 2 Watts, programmable down to 2 mW.

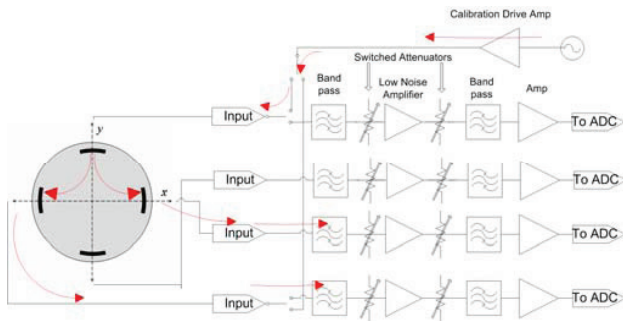

Figure 2: Calibration scheme block diagram.

Output Limiter

An unwelcome feature of the high dynamic range amplifiers in the signal channels is that the potential output power levels can overdrive the ADC inputs to damage. The AFE board contains fast comparators that shut down the outputs as an overvoltage is approached.

Control

A Xilinx FPGA controls programmable attenuators, generates the timing sequences for the calibrator and limiter, and communicates with the processor on the AFE board via a QSPI (queued serial peripheral interface) link.

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ADC BOARD

The digitizer board, developed for LCLS low-level RF control, carries four Linear Technology Corp. LTC2208 16-bit ADCs sampling at 120 MHz. We expect about 12.4 effective bits on a 140 MHz signal. Since the input signal frequency is higher than the sampling frequency, the ADC under-samples the data, aliasing the 140 MHz signal to 20 MHz, and the 200 MHz signal to 40 MHz. A processor on the board transmits ADC waveform data over a dedicated network link (Fig. 3) to a local VME processor which calculates beam charge and position and makes these data available to EPICS [2]. A separate network links the ADC board processor to the accelerator network for configuration and control.

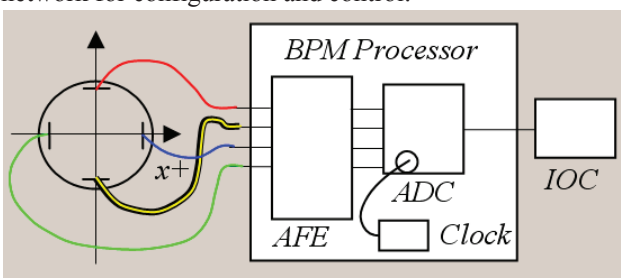

Figure 3: BPM system block diagram.

RESOLUTION

We evaluate BPM resolution in the presence much larger beam jitter by acquiring position synchronously over many beam pulses from many BPMs (Fig. 4). We use a least-squares fit to shot-by-shot beam position in each BPM as a linear combination of those measured in the other BPMs. Using 17 of the LCLS stripline BPMs over 120 consecutive beam pulses we find an average position resolution of 4.8 microns rms at a bunch charge of 220 pC. Figure 4 shows pulse-by-pulse measurement of beam position at one particular BPM, the X and Y positions measured there versus those predicted by the best-fit linear combination of 16 other BPMs, and the X and Y positions with the predicted beam jitter subtracted. The scatter of the measured position after beam jitter subtraction is an estimate of BPM resolution.

STRIPLNE BPM DIAGNOSTIC PANEL

The BPM diagnostic panel shows the beam position, attenuator settings, waveforms, and calibration parameters. Figure 5 shows the beam position information while Figure 6 shows calibration data acquisition.

The calibrator display shows the raw calibration waveforms, the measured gain ratios, and the calibration tone attenuator settings.

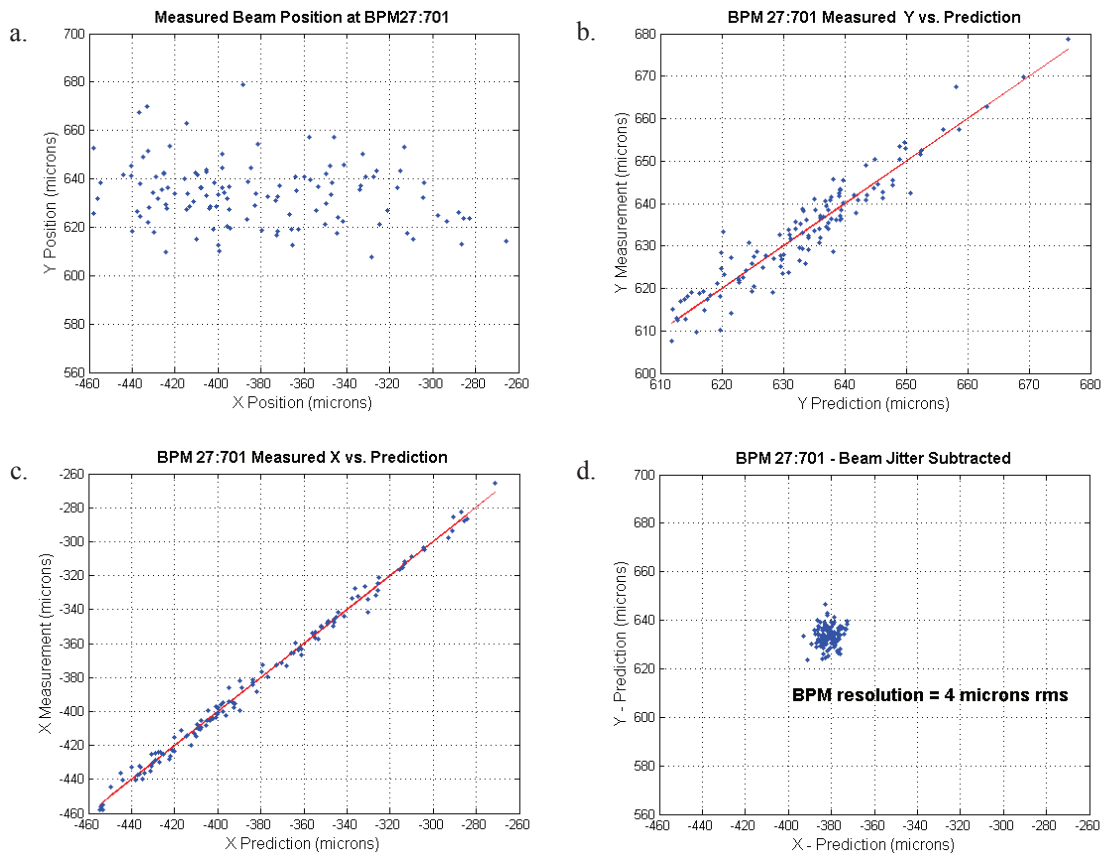

Figure 4: (a) X, Y position measured at BPM 27:701, (b) Measured Y versus Y predicted here from 16 other BPMs, (c) Measured X versus X predicted here from the other BPMs, and (d) X, Y with the beam jitter removed.

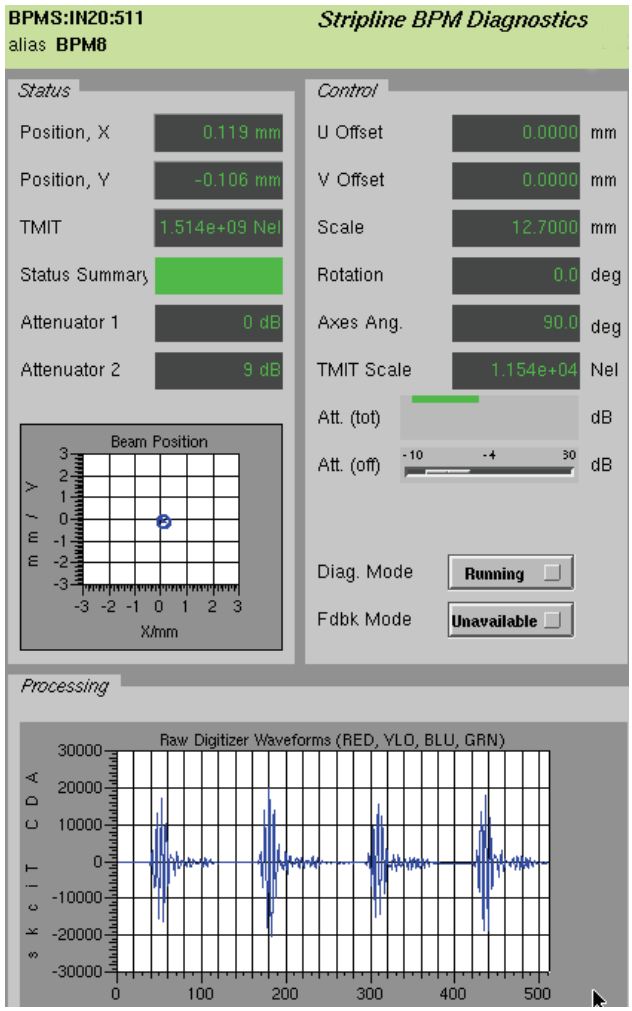

Figure 5: BPM diagnostics panel, beam position.

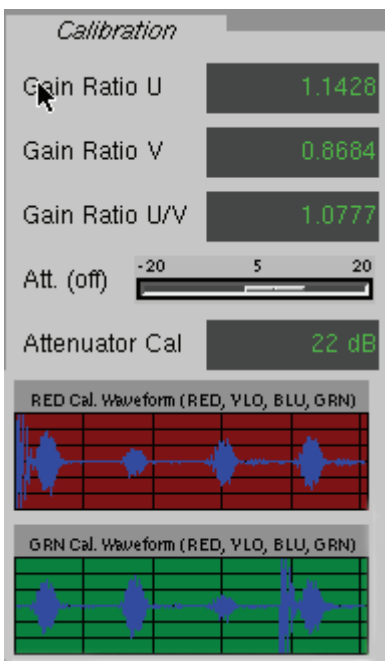

Figure 6: BPM calibration data.

BPM Installation

The LCLS contains 179 BPMs. Of these 83 are striplines served by this new processor (see Figures 7 and 8), 60 are striplines served by older electronics, and 36 are RF Cavity BPMs described in Reference [3].

Figure 7: BPM processors in the rack, front and back.

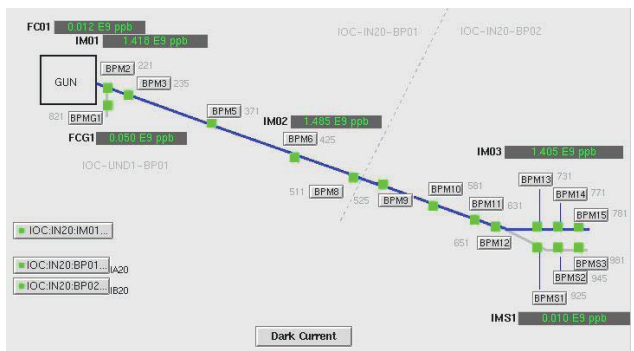

Figure 8: BPMs installed in the LCLS injector.

SUMMARY

Eighty-three of new digital BPM processors have been installed and tested. Single-shot resolution, better than 5 microns rms at 200 pC, has been demonstrated.

REFERENCES

[1] E. Medvedko et al, "Stripline Beam Position Monitors For LCLS," Proceedings of BIW08, Lake Tahoe, California, May 2008.

[2] T. Straumann et al, "LCLS Beam-Position Monitor Data Acquisition System", Proceedings of ICALEPCS07, Knoxville, Tennessee, USA.

[3] S. Smith et al, "Commissioning and Performance of the LCLS Cavity BPM", these Proceedings.